Impact of Ports Reference Choice on S-Parameter Modeling of BGA Package Interconnections

Marco Occhiali
Ansys Customer Excellence,
Electronics EMEA SIPI Team
Ansys Italia
Milano, Italy
marco.occhiali@ansys.com

Aurora Sanna
Back-end Manufacturing and
Technology R&D
STMicroelectronics
Agrate Brianza, Italy
aurora.sanna@st.com

Flavia Grassi
Dept. of Electronics, Information and
Bioengineering
Politecnico di Milano
Milano, Italy
flavia.grassi@polimi.it

***Abstract*—In the context of integrated circuits (ICs) development, package electrical modeling is a fundamental task for die-package-board system optimization. On high-speed digital devices, Ball Grid Array (BGA) package platform is often the preferred choice thanks to its layout flexibility, and S-parameter modeling approach provides the most accurate broadband description of this kind of structure. Since package S-parameters have a very small variation range, they are highly sensitive to extraction inaccuracy due to intrinsic setup approximations, and this effect becomes stronger when frequency increases. This paper is focused on a particular aspect of S-parameters extraction setup, that is the reference node definition for the ports applied in the extraction environment. Different methodologies are described, in the attempt to analyze and quantify their impact on the S-parameters. After a deep investigation regarding stand-alone package interconnections, effects on a complete system are evaluated.**

Keywords—S-parameters, BGA, Package, Pin group, Port.

I. Introduction

To model the parasitic effects of electrically-long interconnections such as cables or PCB traces, S-parameter extraction obtained by full-wave simulation is a widely used methodology. With the increasing frequencies of digital applications, this approach is spreading also in the context of IC-packages, gradually replacing the traditional technique based on lumped RLC elements [3]. In this framework, the extracted S-parameters are the starting point to generate macro-models for circuit simulation, in addition to represent reflection, transmission and crosstalk losses of a passive network. The S-parameters extraction techniques used for complex BGA (Ball Grid Array) packages mostly derive from PCB modeling framework and use the same commercial tools, based on hybrid solvers and 2.5D approximation; in particular, the tool used for the extractions is Ansys SIwave [5], [6], [7]. Package interconnections are typically much shorter than PCB interconnections. Consequently, typical losses values are reduced and target thresholds become lower. In this scenario, a small error in the S-parameters behavior due approximations in the extraction setup acquires a larger weight, representing a larger percentage of the reference quantities.

A typical S-parameter characterization is carried out by extraction tools by setting up a port between the terminals of the interconnection (i.e., the signal forward path) and a reference point, which constitutes the terminal of the current return path [6]. Ports are usually fictitious circuit elements used to apply an excitation (in the cases analyzed in this work, current sources are exploited) to the structure in a specific position. The advantage of simulation, compared to measurements, is that all positions are allowed, including those that are usually not accessible in the actual structure.

The described generic setup can be applied to a signal interconnection designed in a Flip-Chip BGA package [1]. An example is presented in Fig. 1 that shows, in dark blue, a point-to-point signal interconnection between a single bump (die side, top layer) and a single ball (PCB side, bottom layer). The bump and the ball constitute the two ends of the signal forward path. The return path is instead represented by the ground net, in brown, that includes large copper planes and multiple dedicated pins both on the top layer (bumps) and bottom layer (balls). A typical ground interconnection offers multiple return paths to the signal currents flowing through it. To run a S-parameter extraction of the described structure, ports must be applied to the signal nets and referenced to the ground net as depicted in Fig. 1. Based on what explained, there is not a unique choice for reference pins, but multiple options. The actual current distribution depends on the electrical properties of the overall return path including the package, the PCB and the die. Since the current will preferably flow through those paths offering the lowest impedance [2], it is hard knowing beforehand the actual current distribution. This is especially true when working at package level, since die and PCB configurations are often not available or not unique. Moreover, the impedance variations with frequency contribute to problem complexity.

In selecting the reference ports, two main approaches, both based on some approximations, are common. The *nearest pin* method consists in assigning to each signal pin the nearest ground pin available in the layout. Conversely, the *pin group* method uses a fictitious reference node represented by a group of ground pins, that are forced to be at the same potential. Working on BGA packages, resorting to one of these approaches rather than to the other introduces non-negligible differences in the S-parameters behavior, especially at high frequencies. Since the actual current distribution is not predictable, a possible approach is to quantify these differences and identify the worst-case approach for each parameter of interest. Then, if the parameter is within its target value in the worst-case scenario, this will guarantee a good performance of the actual device. The following sections analyze, by means of examples, the impact of different referencing options on the S-parameters of a real BGA layout. The investigation is focused on the ports placed on the ball side, which are more critical than the others. Indeed, the average distance among balls is often comparable with the overall interconnection length.

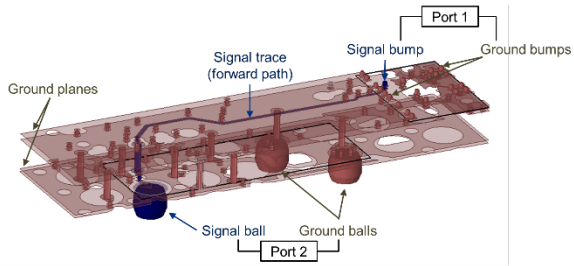

Figure 1: Ports setup for a BGA package interconnection.

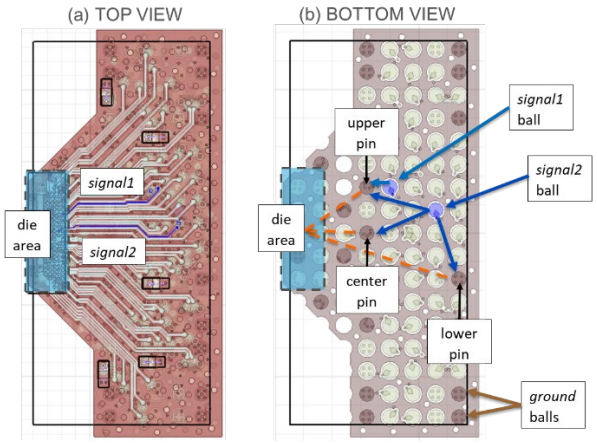

Figure 2: Package layout: (a) top view with highlighted signal nets; and (b) bottom view with highlighted signal balls and nearest pin reference options.

Hence, the choice of the reference node has a significant impact on the resulting current loop, and consequently on the resulting losses. Conversely, on the bump side, the negligible pin-to-pin distance leads to less significant differences.

II. Single Pin Reference: Nearest Pin Approach

The analyzed test case is a layout portion of a 6-layer Flip-Chip BGA substrate, dedicated to the routing of a high-speed digital interface including signal, power and ground nets. Two signal interconnections (named *signal1* and *signal2)* are considered, in order to analyze both self and mutual S-parameters. The signal paths from the top to the bottom layer are highlighted in blue in Fig. 2(a). They consist of traces and vias, and represent the forward paths for the current. The return path is offered by the ground net (in brown color in Fig.2). The current distribution through this complex structure depends on the current injection points, which correspond to the reference nodes assigned to the ports. As shown in Fig.2(b), multiple balls are available as options. Since AC currents tend to follow the minimum impedance path, i.e., the path associated to the minimum inductive loop area, a preferred return path as close as possible to the forward path is expected, [2], [3]. An immediate reference choice for a signal pin is then the nearest ground pin available on the grid. Extraction tools often allow setting this choice automatically, to help the user and speed up the extraction process. However, mindlessly applying this criterion might not be ideal in every situation.

For this analysis, two signal balls with a peculiar position in the ball grid array are chosen, as shown in Fig. 2(b). The former one, i.e., the *signal2* ball, has three ground balls at the same distance, so that there is not a unique choice satisfying the nearest pin criterion. Indeed, three approximate current paths followed by the current, in order to reclose right below the die (left side of Fig. 2(b)), can be identified, which are highlighted as orange dashed lines in Fig. 2(b). Conversely, the latter ball, i.e., the *signal1* ball, has a very clear choice for the nearest pin as reference, that is the *upper pin* in Fig. 2(b). This reference will be kept constant throughout this analysis, while *signal2* port settings will change. More in detail, *signal2* has three possible approaches: (a) a ball close to the most direct path towards the die, coincident with the one for *signal1* (*upper pin*); (b) a ball close to the most direct path towards the die, but not the same as *signal1* (*center pin*); (c) a ball far from the most direct path possible towards the die (*lower pin*). From now on, the above presented candidate pins will be referred to as *upper pin, center pin* and *lower pin*.

A. Impact on Reflection and Transmission Losses

Fig. 3 compares the bump to ball transmission coefficient of *signal2* for the three different reference choices. This parameter is typically used to represent and evaluate the transmission losses of an interconnection. Choosing the *lower pin*, which is the furthest from the trace path, forces the current through the largest loop, resulting in a worsened profile. In particular, supposing a -1 dB threshold, which is a typical requirement for many digital applications, this choice crosses the limit line nearly 2 GHz before the others, thus reducing the overall bandwidth in which the connection performance falls within the 1 dB loss target. The other two pins give pretty similar losses profiles, which is consistent with the fact that the corresponding return paths involve a smaller current loop with respect to the path associated with the *lower pin*. Similar considerations are valid for reflection coefficient. Furthermore, the difference among curves increases with frequency (as it becomes particularly evident for frequencies above 5 GHz).

B. Impact on Crosstalk

In order to analyze the impact on crosstalk, mutual S-parameters between *signal1* and *signal2* terminals are considered. The curves in Fig. 4 describe the coupling from *signal2* bump (aggressor) to *signal1* ball (victim), that is the far-end crosstalk. This parameter is not directly influenced by the size of the current loop, but mainly by the presence of a common return path shared among different signals. In particular, if the same reference (*upper pin*) is chosen for both signals, the common portion of return path is maximized, thus resulting in the maximum mutual interaction (red curve). The reference choice for *signal2* ensuring the least crosstalk is the *lower pin*, which is the furthest from the reference of *signal1* (*upper pin*): this grants as much decoupling as possible of the two return paths. Similar results, omitted here for brevity, were obtained also for the near-end crosstalk.

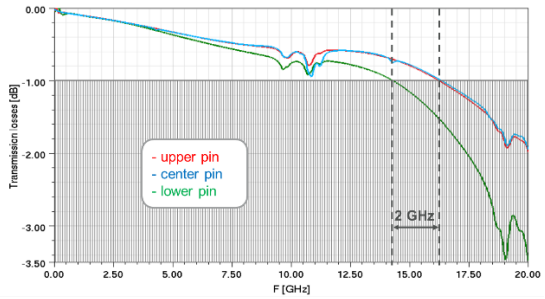

Figure 3: Signal2 transmission coefficient at varying reference pin.

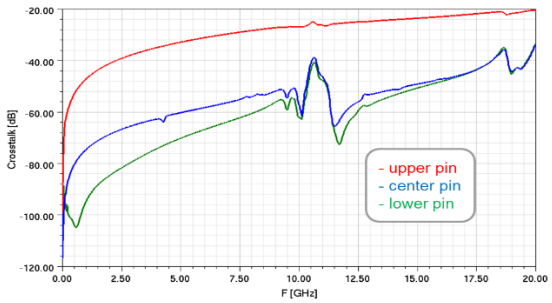

Figure 4: Far-end crosstalk from signal2 to signal1 for three possible choices of the reference pin for signal2.

In summary, the choice of the *lower pin* as reference for *signal2* represents, at the same time, the worst-case for transmission and reflection losses and the best-case for crosstalk.

III. Pin Group Reference Approach

Choosing a single reference pin might be a stretch in terms of actual physical behavior. If a single ground pin very close to a signal pin exists, it makes sense to assume that the return current will mostly flow through it. Conversely, if there is not an immediately close ground pin, or if there are several at the same distance from the signal line terminal, it would be inaccurate and arbitrary to force the current flowing through a specific one. A solution is to resort to a group of pins as reference for all signals. The drawback of this approach is that all pins in the same group are forced to be exactly at the same potential. This is clearly not realistic, but it offers more degrees of freedom to the simulated currents in their distribution among multiple paths. The pin group can have different sizes and positions with respect to the trace path. These two aspects will be analyzed independently in the following sub-sections.

A. Impact of the Pin Group Size

To investigate the impact of the size of the pin group, a group of ground balls roughly centered around the signal paths is here considered as reference for both *signal1* and *signal2* ports. For simulation, group dimensions with progressively increasing size are exploited (see Fig. 5). More specifically, the *small group* includes four balls, the *medium group* includes thirteen balls, the *full group* includes all the available twenty-three ground balls.

Fig. 6 shows transmission coefficient of *signal1* at varying group dimensions. The three grouping options are also compared to the nearest pin reference that is the pin immediately close to *signal1* ball (*upper pin*). Indeed, single pin is an extreme case corresponding to the smallest possible group and, in this specific situation, forces the smallest possible current loop. The plots clearly indicate a trend: eenlarging the group worsens the losses, because part of the current flows through paths that are far from the signal trace. However, the most significant variation is observed between the single pin and the *small group* cases, that cross the – 1dB threshold at 1 GHz distance. When the group is furtherly enlarged, the difference in performance decreases and tends to zero (*medium group* and *full group* curves are almost overlapped), since the portion of current flowing through peripheral paths becomes negligible. Although not shown here for brevity, reflection coefficient exhibits a similar behavior.

Fig. 7 shows the far-end crosstalk from *signal2* bump to *signal1* ball. Thanks to the spread of the return currents among multiple paths, enlarging the group has the effect to decrease crosstalk. A small pin group, instead, forces the two return currents to share a low number of pins and therefore maximizes the overlapped return paths, increasing the mutual interaction. The upper limit is given by the smallest possible group, that is a single pin taken as reference for both signals. Two separated single pins, instead, minimize the coupling between return paths.

As already mentioned for the nearest pin approach, two opposite trends are observed: A small group provides the best transmission and reflection losses, but the worst crosstalk.

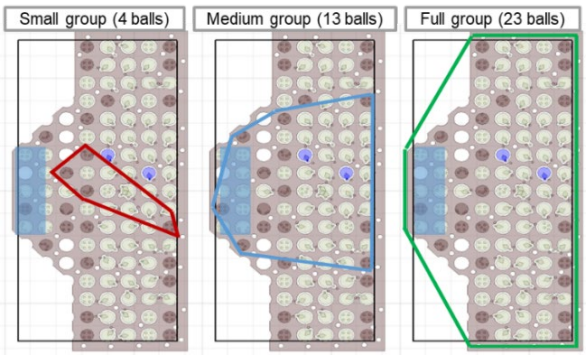

Figure 5: Different pin-group configurations with increasing size.

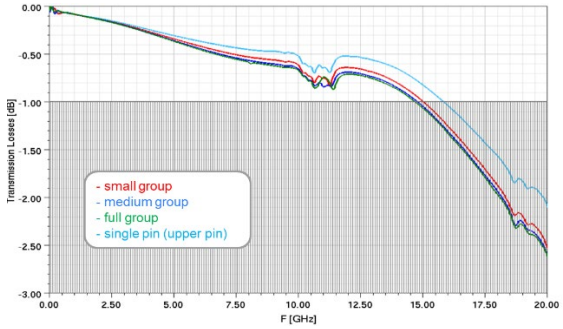

Figure 6: Signal1 transmission coefficient at varying pin group size.

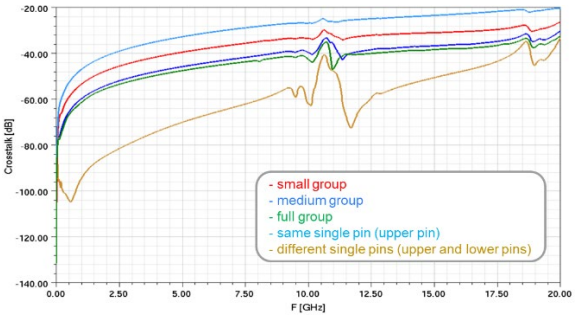

Figure 7: Impact of pin group size on crosstalk.

B. Impact of Pin Group Position

This section investigates the effect of varying the group position with respect to the signal path. Fig. 8 presents the analyzed configurations. Each group is placed between the signal balls and the die area. The *centered group* includes the three ground balls that are closest to the traces path. The *elongated group* is larger and has its center shifted towards the south layout region. The last group includes the *lower pin* presented in Section II, which is very far from the traces path.

If *signal2 is considered,* Fig. 9 shows that the *centered group* offers the best transmission performance, also well overlapped to the single reference pin case, if the *upper pin* is chosen. This is not surprising, since the considered group is very small and close to the *upper pin* area. As the group gets less centered on the trace path, losses get worse. Indeed, the *elongated + lower pin group* is the grouping option closest to the worst scenario, represented by the single pin reference if the *lower pin* is chosen. This demonstrates that including in the group an "off the trace" pin, negatively affects losses, but not as much as only considering a far pin singularly. It should be highlighted that although the *elongated + lower pin group* includes less balls than the *elongated group* (eight vs nine), it exhibits a worse behavior. This means that the considerations in Section II-A are valid as long as the size variation does not significantly change the barycenter of the group. If the group

position with respect to the trace path is modified, the number of pins is not sufficient to predict the final behavior.

Reflection coefficient behaves similarly to transmission coefficient, but crosstalk (Fig. 10) shows again the opposite trend. Less crosstalk is observed if the reference group gets progressively spread further away from the trace path. This confirms that pin grouping is an intermediate option between the best and the worst case represented by a single reference pin, respectively different or the same for the two signals.

IV. From Package Level to System Level

So far the presented analysis was focused on stand-alone packages only, but the impact on a system-level analysis also including die and PCB models should be mentioned. The curves in Fig. 11 represent the transmission coefficient from the package bump of a signal driver to the input pad of a signal receiver placed on the PCB. Plots refer to *signal2* and were obtained by cascading the S-parameter models of the package with the S-parameter model of a test board. Each plot represents one of the referencing options described in the previous sections, applied both for package and PCB model extraction.

It can be observed how the differences between the considered options become less significant, if compared to the order of magnitude of the full system losses.

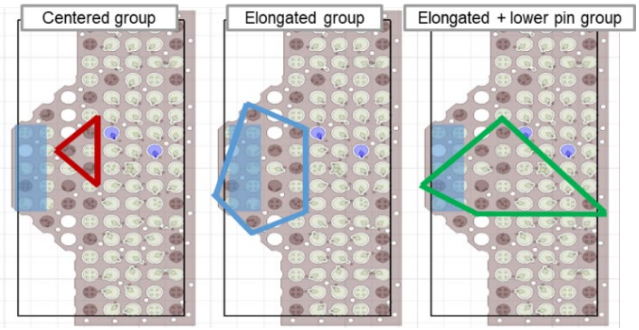

Figure 8: Pin group configurations with different positions.

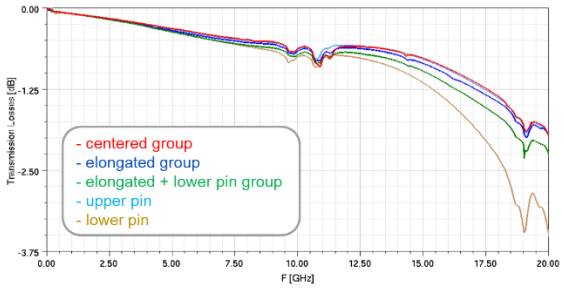

Figure 9: Signal2 transmission coefficient at varying pin group position.

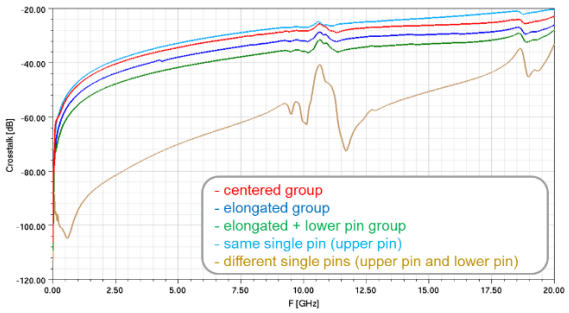

Figure 10: Impact of reference position on crosstalk.

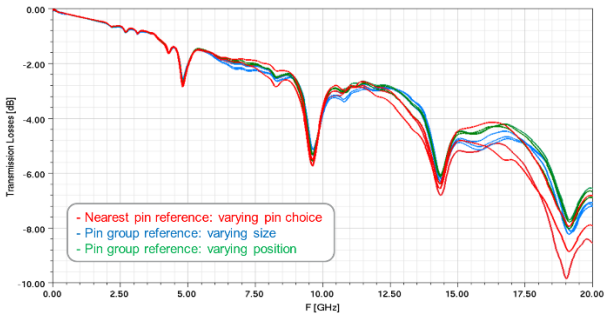

Figure 11: Package + PCB transmission coefficient.

This translates into a negligible impact on the time-domain signal waveforms obtained when a digital signal source is injected in the system and monitored on a matched load.

This demonstrates that a deep understanding of the ports referencing effect is of paramount importance as long as package parameters are evaluated stand-alone. Conversely, this does not significantly impact on system-level analysis.

V. Conclusions

In this work, guidelines were provided to understand the impact of ports referencing on the performance of the S-parameter model of a BGA package interconnection. It has been demonstrated that a reference node (pin or group) closer to the signal forward path and concentrated in a small area provides optimal reflection and transmission performance at the price of increased crosstalk, if the same reference is shared with other signals. On the other hand, spreading the reference over a big group or placing it far from the signal path reduces crosstalk but significantly worsens transmission losses. This allows identifying the worst-case setup based on the most critical parameter in the design, in order to ensure its optimization in the most challenging scenario. Besides the simulation methodology aspects, significant guidelines can be also derived for package design and ball-out definition, since the impact of the ground balls distribution on the overall interconnection behavior is implicitly described. These aspects may become critical as long as the objective is to predict the performance of stand-alone packages, but become negligible when the package is included and simulated in a system-level environment.

References

[1] G. Graziosi, C. Somma, A. Sanna, “BGA Package Design Techniques for Electrical Performance Awareness,” in Proc. MiNaPAD Conference, Grenoble, 2017.

[2] S. Caniggia, F. Maradei, “Signal Integrity and Radiated Emission”, Wiley, Chichester, United Kingdom, 2008.

[3] Clayton R. Paul, “Introduction to Electromagnetic Compatibility”, Wiley, United States of America, 1992.

[4] B. Young, “Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages”, Prentice Hall, Upper Saddle River, USA, 2000.

[5] ANSYS Inc., “SIwave 2020R1 Online Help”, Canonsburg, PA, 2020.

[6] E. Bracken, S. V. Polstyanko, “Coupled thermal-fluid-electrical simulation for printed circuit board design”, in Proc. ICEAA Conference, San Francisco, United States of America, 2011

[7] D. Soldo, S. G. Pytel, “Automated Decoupling Capacitor Analysis for Analog/Digital Printed Circuit Boards”, in Proc. EMC Compo Conference, Dubrovnik, Croatia, 2011