Control and Fault Analysis of Multiport Converters for Low Voltage DC Distribution Systems

Simone Negri[a], Enrico Tironi[a], Gabrio Superti-Furga[a], Giovanni Ubezio[b]

[a] Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, piazza Leonardo da Vinci 32, 20133, Milano, Italy

[b] Energy Components & Consulting S.r.l., Via Santa Petronilla, 7, 23889 Santa Maria Hoè (LC), Italy

E-mail addresses: simone.negri@polimi.it, enrico.tironi@polimi.it, gabrio.supertifurga@polimi.it, giovanni.ubezio@gmail.com.

***Abstract*—The recent evolution of distribution systems has shed light on innovative solutions aimed at enhancing the performance of such systems. In this paper, the authors focus their attention on two modular, non-isolated multiport DC/DC converters and their application to low voltage DC distribution systems. The first topology is based on a capacitive internal link, while the second one is based on a less usual inductive link. Unconventional control strategies based on a lower-level pseudo-sliding mode control algorithm and a higher-level control based on inverse dynamics are proposed for both topologies by means of a general, fully modular control design. A six-port application is discussed in detail and its operation is analyzed in steady state, under abrupt load/generation changes and in case of pole-to-pole faults. Finally, a systematic comparison between the two topologies is performed.**

***Keywords*—DC/DC converters; distributed generation; LVDC distribution; multiport converters; smart grids.**

1. Introduction

Distribution grids are undergoing heavy changes. Diffused generation is getting more and more widespread, with many power electronics devices being connected to the grid [1], [2]. In addition, most of these devices require a preliminary AC/DC conversion stage, and their power quality and continuity features need to meet increasingly demanding standards. A common approach found in different studies is the subdivision of power systems in active subsystems [3] - [9] coordinated by a common high level supervisor [10] - [13]: this allows not only obtaining better performances in terms of system regulation, but also considering islanded operation of some portions of the system [4] - [8].

These considerations, along with technological progress in matter of storage devices and power electronics converters, sparked new interest on DC distribution systems. Among many different system architectures, Multiport Converters (MCs), possibly with integrated electronic transformers, are considered with particular attention [14] - [35]. Those converters are particularly useful when it is necessary to interface different energy sources, storage devices and loads with one integrated topology [18], [20], [23], [25] - [27], [30], while the traditional approach would require many two-port converters. The introduction of MCs allows reducing dimensions and costs and enhancing efficiency [24] - [32]. The centralized control allows obtaining better system dynamics and higher power quality and continuity [9], [18] - [24], [32]. Among the many studies available, two main categories are recognizable: MCs based on a capacitive internal bus [18] - [23] and MCs based on an inductive internal bus [23] - [35]. The second category is then split among three sub-categories: isolated MCs [24], [25], [30], [31], non-isolated MCs [33] - [35] and MCs with a mix of isolated and non-isolated ports [26] - [28], [32]. Furthermore, considering the wide range of possible applications, some MCs exhibit modular topologies [18] - [23], [33] - [35], while others are designed with a specific number of ports and are not easily expandable [24] - [32]. From the control point of view, most MCs controls are based on voltage modulation techniques, often based on commutation phase-shift control [24] - [32], which is mandatory for isolated converters comprising a high-frequency transformer. Some other studies, on the contrary, base their control algorithms on mean-value quantities [18] - [20], [33] - [35], manipulating the duty-cycle through suitable current and voltage loops. Finally, only few papers consider the converter behavior and control under external or internal fault condition [9], [20], [23], [35].

Considering the application of MCs to Low Voltage DC (LVDC) distribution systems, some issues are still open: all the aforementioned examples have proven to be effective for their specific application, but it has not been fully discussed whether they are suitable for extensive distribution system applications. In particular, a modular architecture seems to be of the utmost importance for distribution systems applications, but this issue is often overlooked: in [33] a three-port inductive-link converter is discussed and its advantages in efficiency and in avoiding bulky capacitors are recognized, at the expense of higher control complexity and implementing effort. Furthermore, it has been pointed out that it is not easy to extend the number of ports. In order to overcome such limitations, a first study has been presented in [23]. In fact, for this specific application different topologies should be compared and evaluated considering components, control algorithms and fault behavior.

In this paper, the authors focus their attention on the application of multiport converters to DC distribution systems. Two different topologies are selected and investigated: the first topology, characterized by a capacitive internal bus, has been discussed in [18], while the second one, characterized by an inductive DC bus, has been proposed in [33]. The general aspects and features of the selected topologies are presented and innovative control strategies are developed for both topologies

by means of a general control design approach which is fully modular, with a non-preassigned number of ports. The proposed control, based on a direct current-tracking approach, allows for higher dynamic performances and an easier control synthesis; in addition, it can be homogeneously applied to both topologies, leading to a meaningful comparison. In the subsequent application, a specific number of ports is assumed, each one with its own functionality, and control laws are provided to obtain effective control in presence of storage devices and renewable energy sources. Converters operation is analyzed in steady state, under abrupt load/generation variations and in case of pole-to-pole faults on a port and on the internal bus in order to highlight the strengths and weaknesses of the selected MCs.

Three main contributions for MCs applications are introduced. Firstly, the control of both the selected topologies is based on a two-layer structure, where a pseudo-sliding mode control is applied to Power Electronics Building Block (PEBB) currents and an inverse dynamic control approach is applied to voltage controllers design. Pseudo-sliding mode current controllers are appreciated for their wide dynamic band, stability and robustness, besides deeply simplifying reorganization of the control design [36] - [41]. The second contribution concerns MCs with inductive internal bus, which would require more complex control methods when using voltage modulation approaches [33], [34]. This paper shows that it is possible to extend the pseudo-sliding mode current tracking control also to MCs with inductive internal DC bus, overriding its well-known drawbacks in complex systems due to interferences between switched currents [34], [37], [42], [43] and with no need to measure the internal bus voltage, in contrast with [34]. Lastly, in order to overcome the lack of effective circuit breakers, which represents a traditional issue of DC systems, the proposed control approach is developed with a particular attention to current controllability during faults. Consequently, the converters are tolerant with respect to external faults and can be integrated in system protection [9].

This paper is organized as follows: Section 2 illustrates the considered MC topologies and control principles, while Sections 3 and 4 report the modulation design of the first and second topology, respectively. An application to LVDC systems and its related control is presented in Section 5, while the related dynamic modeling and stability analysis is reported in Section 6. Fault analysis and simulation results are reported in Section 7 and 8, respectively. In Section 9 a comparison between the two examined topologies is performed and final conclusions are provided in Section 10.

2. Multiport Converters Topologies and Control Principles

A general N-port MC scheme consists of N I/O converters, which can be constituted by a single PEBB, each one representing one of the converter ports. An IGBT-based PEBB scheme is reported in Figure 1. In general, it is possible to realize a compact, physically protected DC-bus with relatively long connections to loads or, on the contrary, an extended DC-bus with short and physically protected load connections. Further considerations, presented later in this paper, will show the advantages and disadvantages of each of these approaches.

The first selected topology is shown in Figure 2. Differently from [18] - [23], diodes are connected in parallel to each port capacitor, such that, in case of external faults, voltage across the capacitor cannot become negative [9]. This would lead to capacitor damage and loss of controllability, which will be discussed later on. The second topology is shown in Figure 3. Note that, in this second topology, there is no need for external diodes because that protection function is naturally performed by the PEBB free-wheeling diodes. For both topologies the overall MC control is constituted by two layers: the lower one is constituted by the pseudo-sliding mode control of PEBB currents, while the higher control layer, which should provide suitable current references for the lower one, is based on an inverse dynamic approach.

The basics of sliding mode control and its effectiveness in power converters control are well-known in literature [38], [39], [44] - [46]. In particular, the fundamental principle of this control approach is to force to zero a function of the system states, called sliding function, by means of a discontinuous on-off-style control law. When a sliding mode is enforced, the sliding function is null except for high-frequency ripple and the system is considered in sliding condition. While in sliding

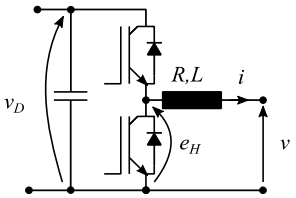

Figure 1 - PEBB as I/O converter

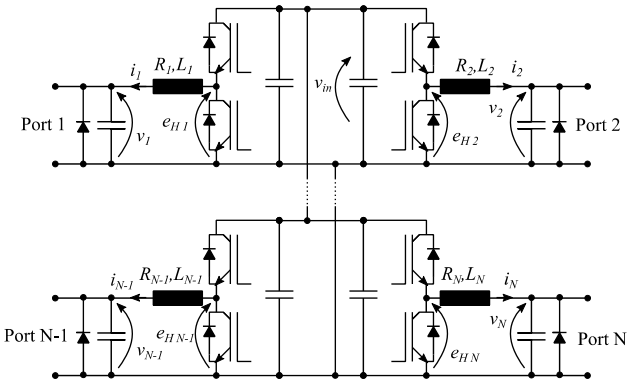

Figure 2 - First MC topology

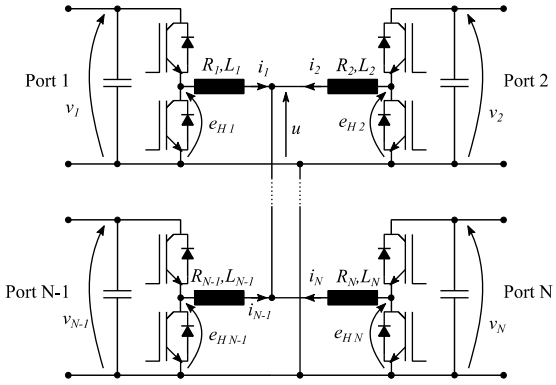

Figure 3 - Second MC topology

condition, the system is characterized by specific properties (i.e. linearity, reduced order and assigned dynamics). If, for any reason (i.e. system start or macroscopic disturbance) the sliding variable becomes non-null at a certain time, the control design would force this variable to zero in finite time. The phase in which the sliding variable is forced to zero from a non-null initial value is called reaching condition. However, a significant issue is often encountered when designing sliding-mode controllers for power converters, in that, from a theoretical perspective, the switching frequency should be ideally infinite and, practically, as high as possible. This is clearly in contrast with power converters design, where the switching frequency is chosen as a trade-off between dynamic performance and reduction of current harmonics on the one hand and cooling system and semiconductor device limitations on the other hand. In addition, for power converters applications it is desirable to have a constant switching frequency. In order to address this issue, the most common approach is to determine a control law which ensures that the controlled states are maintained in an assigned band centred around the sliding manifold, such that a pseudo-sliding (or quasi-sliding mode) mode is enforced [39], [43], [47].

The inverse dynamic technique is ascribable to the feedback linearization family [45], [46] and is largely applied in robot manipulators control [48]. It is based on the introduction of a suitable feedback such that the original (nonlinear) Multi-Input-Multi-Output coupled system is transformed into a set of linear, possibly decoupled systems with assigned dynamics. Similar approaches are recognized in sliding manifold design, with particular reference to integral sliding mode control [45]. In the following, the inverse dynamic is introduced since the relative order of the controlled system is larger than one, such that a higher-order sliding mode controller would be necessary to enforce a sliding mode on the controlled states. The introduction of a higher-order sliding mode controller would require a significantly more complex control design in order to consider systems constraints [49], such as semiconductors maximum current. However, the properties of linearity, reduced order and assigned dynamics of a system in sliding condition are desirable in this application. Consequently, the inverse dynamic is introduced to relate the controlled states, which cannot be directly controlled by means of a sliding mode controller, to the states on which a pseudo-sliding mode can be easily enforced. The general approach adopted for lower-level modulation design also allows developing a totally modular control structure, with no need for predetermined port functionalities or number of ports.

3. First Topology: Modulation Design

In this paper, a pseudo-sliding mode control has been selected for its superior dynamic performances, robustness and simplicity. Referring to Figure 1 for symbols, assume the inductor to be linear and let i^* be the reference current for the modulation algorithm. Consider the sliding function (inductance flux error) λ defined as

$$\lambda = L(i - i^*) \tag{1}$$

Let f_{sw} be the switching frequency and, consequently, $T_{sw} = 1/f_{sw}$ be the designed switching period. In addition, assume the following:

- positive DC bus voltage: $v_D > 0$
- negligible resistive terms on high-frequency ripple: $R << 2\pi f_{sw} L$
- quantities v_D, v and i^* being suitable, Lipschitz-continuous functions with spectra limited to frequencies much lower than the switching frequency f_{sw}.

Referring to Figure 1 and considering the inductor constitutive equation, the relation between the sliding function λ and the ideal switched voltage e_H is then formulated as

$$\frac{d\lambda}{dt} = e_H - u_{eq} \tag{2}$$

where e_H is the ideal switched voltage, which has two possible instantaneous values, 0 and v_D. u_{eq} is expressed as

$$u_{eq} = v + L\frac{di^*}{dt} + Ri^* \tag{3}$$

and represents the equivalent voltage, which is defined from sliding mode control theory as the ideal continuous value of the discontinuous control variable e_H necessary to perform the desired control action [47]. Consequently, in sliding condition the equivalent voltage u_{eq} is equal to the mean value of the switched voltage e_H. Note that, when considering the longer time-scale related to mean-value quantities, such as the equivalent voltage u_{eq}, resistive terms are not necessarily negligible.

The controllability condition is determined considering that, to maintain sliding condition, it is necessary to be able to impose positive and negative derivative (2) on the sliding function λ. Consequently, the controllability condition is expressed as

$$0 < u_{eq} < v_D \tag{4}$$

The modulation algorithm used to enforce a sliding mode is based on a dynamic set of slanted thresholds [36], which are conceived to impose the ripple ideal triangular waveform with null average value. Considering now a set of equally spaced time intervals T_k such that

$$T_{k+1} = T_k + \frac{T_{sw}}{2} \tag{5}$$

In each time interval $t \in [T_{k-1}, T_{k+1}]$, the resulting control law is

$$e_H = \begin{cases} v_D & if \quad \lambda < \left(v_D - u_{eq}\right)\left(t - T_k\right) \\ 0 & if \quad \lambda > \left(-u_{eq}\right)\left(t - T_k\right) \end{cases} \tag{6}$$

Equation (6) realizes the system of slanted thresholds proposed in [36]. The resulting control scheme is reported in Figure 4. For clarity, the behaviour of the variables e_H and λ in quasi-stationary conditions is reported in Figure 5. As long as the average power associated with the switching ripple is negligible, the average converted power is given by

$$P = u_{eq} \cdot i^* \tag{7}$$

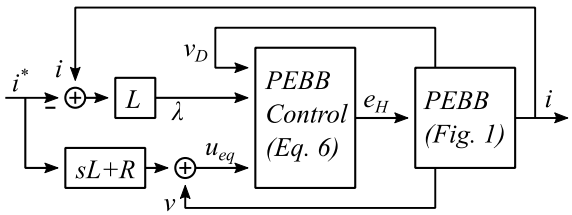

Figure 4 – First topology modulation block diagram

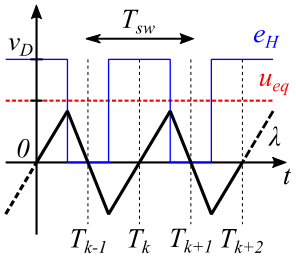

Figure 5 - Ideal local behaviour of the sliding function λ (black), equivalent voltage u_{eq} (red, dotted) and switched voltage e_H (blue)

The proposed algorithm is independently applied to each of the PEBBs realizing the first MC topology, such that it controls the commutations imposing constant switching frequency.

4. Second Topology: Modulation Design

The second topology is characterized by an inductive node on the DC bus and, consequently, the independent PEBB currents are N-1. Considering the system reported in Figure 3, one can note that each PEBB current depends on the difference between the PEBB switched voltage e_H and the internal bus voltage u. However, one can also note that the internal bus voltage is not an independent variable, but can be obtained as a linear combination of the N switched voltages e_H and of the N voltage drops on switching inductances. Consequently, the N-1 independent currents depend only on the N switched voltages. This implies that the modulation algorithm selected for the previous configuration cannot be directly applied to this second one, since it requires independent currents. However, it is useful to introduce a control algorithm such that the N physical currents can be treated as independent, in that this allows for totally modular physical and control structures. Furthermore, as discussed later on in this paper, the proposed approach is suitable to mitigate the effects of external faults.

In the following, a decoupling algorithm capable of managing both aspects of this particular topology is developed, so that the modulation algorithm of the previous Section can be extended. This approach has been proposed in [42] and applied in extended form for control design in complex power converter systems in [37]; a more general and formal discussion is presented in [43]. This approach results in equations similar to (2) for each PEBB, in which (1) and (3) are replaced by a set of N modified independent variables. In addition, the proposed method provides a general approach to manage control degrees of freedom, which is critical in this configuration.

4.1. PEBB Control and Decoupling Algorithm

Consider the internal bus depicted in Figure 3 and refer to the same figure for symbols. According to standard mesh analysis, define **L**, **R** as inductance and resistance branch matrixes and **i**, $\mathbf{e}_H$ as vectors of branch current and switched voltage sources. The considered network has N branches and N-1 independent currents, which constitutes the vector $\mathbf{i}_u$. Define the incidence matrix $\mathbf{A}_{(N,N-1)}$ such that

$$\mathbf{i} = \mathbf{A}\mathbf{i}_u \tag{8}$$

Referring to Figure 3, the terms appearing in (8) can be defined as

$$\mathbf{i} = \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix}_N, \ \mathbf{i}_u = \begin{bmatrix} i_2 \\ \vdots \\ i_N \end{bmatrix}_{N-1}, \ \mathbf{A} = \begin{bmatrix} -1 & \cdots & -1 \\ 1 & & \\ & \ddots & \\ & & 1 \end{bmatrix}_{N\,x\,(N-1)} \tag{9}$$

Note that (9) is only one of the possible choices, since $\mathbf{i}_u$ can be composed of any combination of N-1 currents from **i**. As long as the incidence matrix **A** is reformulated accordingly, any choice is valid and produces the same results. The mesh inductance and resistance matrixes are then defined as

$$\mathbf{L}_u = \mathbf{A}^T\mathbf{L}\mathbf{A}, \ \mathbf{R}_u = \mathbf{A}^T\mathbf{R}\mathbf{A} \tag{10}$$

The mesh inductance matrix $\mathbf{L}_u$ is required to be full rank, since a singular $\mathbf{L}_u$ matrix would imply a short-circuit on the internal bus.

Consider now the reference independent current set $\mathbf{i}_u^*$. With reference to Figure 3, one can note that the internal bus voltage u is common to all PEBBs and corresponds to the voltage v indicated for a general PEBB in Figure 1. Consequently, rearranging the dynamic relations on switching inductances (1) - (3) to include network constraints (8), a set of N-1 dynamic equations involving the independent flux errors $\boldsymbol{\lambda}_u$ is obtained, namely:

$$\frac{d\boldsymbol{\lambda}_u}{dt} = \mathbf{A}^T\mathbf{e}_H - \mathbf{u}_{eq}' \tag{11}$$

where

$$\boldsymbol{\lambda}_u = \mathbf{L}_u\left(\mathbf{i}_u - \mathbf{i}_u^*\right), \quad \mathbf{u}_{eq}' = \mathbf{L}_u\frac{d\mathbf{i}_u^*}{dt} + \mathbf{R}_u\mathbf{i}_u^* \tag{12}$$

Note that the internal bus voltage u does not appear in (11), (12) since it does not correspond to an independent voltage source.

As mentioned, the modulation algorithm discussed in Section 3 cannot be directly applied to (11) for two reasons. Firstly, (11) highlights that the flux errors $\boldsymbol{\lambda}_u$ cannot be independently controlled due to the presence of the coupling matrix $\mathbf{A}^T$. Secondly, the difference between the N switched voltages and the (N-1) independent currents leaves one residual control degree of freedom which is necessary to consider in control design. From a physical perspective, considering system topology, one could argue that this residual controllable variable is necessarily a voltage since, given a set of N-1 independent currents, one common voltage is necessary to have determined power flows. Consequently, the residual degree of freedom is

identified as a suitable common term u_m in all PEBB equivalent voltages.

Let u_m be the mean value over one switching period of the average of the N switched voltages, which, in sliding condition, is simply equal to the average of the N equivalent voltages u_{eq}, namely

$$u_m = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} \mathbf{H}\mathbf{e}_H dt = \mathbf{H}\mathbf{u}_{eq} \tag{13}$$

where $\mathbf{u}_{eq}$ is the vector of the N PEBB equivalent voltages and

$$\mathbf{H} = \frac{1}{N}\begin{bmatrix}1 & \cdots & 1\end{bmatrix}_N \tag{14}$$

The common voltage term u_m is considered hereon as the N-th independent variable, which, as mentioned, ensures determined power flows in the internal bus. Consequently, the N independent variables to be considered in control design are the N-1 elements of $\boldsymbol{\lambda}_u$ and the common voltage term u_m. Note that, however, the numerical value of u_m is largely arbitrary, since, in order to obtain the desired internal power flows, the common voltage term can assume any value in a determined range related to controllability conditions. The limits of the allowed range of u_m and a suitable method to determine its value are presented in the following.

In order to control the common voltage term u_m by means of the switched voltages e_H, it is necessary to introduce an auxiliary sliding variable, named heron as g, designed to have zero mean value over one switching period only when the mean value of the average of the N switched voltages is equal to u_m. Consequently, the auxiliary variable g is defined as the integral error between the switched voltage average and u_m, namely

$$g = \int \left(\mathbf{H}\mathbf{e}_H - u_m\right) dt \tag{15}$$

Differentiating (15) leads to a dynamic control equation in the scalar auxiliary variable g , namely

$$\frac{dg}{dt} = \mathbf{H}\mathbf{e}_H - u_m \tag{16}$$

It is hence possible to define a dynamic system composed of N independent equations obtained from (11), (16), resulting in

$$\frac{d}{dt}\begin{bmatrix}\boldsymbol{\lambda}_u \\ g\end{bmatrix} = \begin{bmatrix}\mathbf{A}^T \\ \mathbf{H}\end{bmatrix}\mathbf{e}_H - \begin{bmatrix}\mathbf{u}_{eq}' \\ u_m\end{bmatrix} \tag{17}$$

Note that $\mathbf{A}^T$ and $\mathbf{H}$ are, respectively, a (N-1)×N matrix and a N-column row vector, such they compose a N×N square matrix in (17). In addition, to ensure controllability this composed matrix is required to be non-singular. Consequently, the submatrices $\mathbf{A}^T$ and $\mathbf{H}$ are required to be full-rank.

In order to obtain a decoupled system, according to standard decoupling procedures [50], the dynamic system (17) is left multiplied by the inverse of the matrix composed by $\mathbf{A}^T$ and $\mathbf{H}$. The latter is obtained by means of the auxiliary matrices $\mathbf{K}_{(N,N-1)}$ and $\mathbf{G}_{(N,1)}$, which are defined to satisfy the condition

$$\begin{bmatrix}\mathbf{A}^T \\ \mathbf{H}\end{bmatrix}\begin{bmatrix}\mathbf{K} & \mathbf{G}\end{bmatrix} = \mathbf{1}_N \tag{18}$$

where $\mathbf{1}_N$ represents a N×N identity matrix. Condition (18) is satisfied if

$$\mathbf{A}^T\mathbf{K} = \mathbf{1}, \;\; \mathbf{H}\mathbf{G} = 1 \tag{19}$$

$$\mathbf{A}^T\mathbf{G} = \mathbf{0}, \;\; \mathbf{H}\mathbf{K} = 0 \tag{20}$$

Auxiliary matrices $\mathbf{K}$ and $\mathbf{G}$ are hence obtained from (19) as the right-type, Moore-Penrose inverse of, respectively, $\mathbf{A}^T$ and $\mathbf{H}$, namely

$$\begin{aligned}\mathbf{K} &= \mathbf{A}(\mathbf{A}^T\mathbf{A})^{-1} \\ \mathbf{G} &= \mathbf{H}^T(\mathbf{H}\mathbf{H}^T)^{-1} = \begin{bmatrix}1 & \cdots & 1\end{bmatrix}_N^T\end{aligned} \tag{21}$$

Considering (9), (14), it is easy to verify that the auxiliary matrices $\mathbf{K}$ and $\mathbf{G}$ satisfy condition (20). In addition, the square matrix [$\mathbf{K}$ $\mathbf{G}$] is the inverse of square matrix composed by $\mathbf{A}^T$ and $\mathbf{H}$ appearing in (17).

The desired decoupled system is hence obtained left-multiplying the dynamic system (17) by [$\mathbf{K}$ $\mathbf{G}$], which results in

$$\frac{d\boldsymbol{\lambda}}{dt} = \mathbf{e}_H - \mathbf{u}_{eq} \tag{22}$$

where

$$\boldsymbol{\lambda} = \mathbf{K}\boldsymbol{\lambda}_u + \mathbf{G}g \tag{23}$$

$$\mathbf{u}_{eq} = \mathbf{K}\mathbf{u}_{eq}' + \mathbf{G}u_m \tag{24}$$

The dynamic system (22) is constituted by a set of N independent modified flux errors $\boldsymbol{\lambda}$, such that each variable can be controlled by means of one switched voltage.

The sliding function vector $\boldsymbol{\lambda}$ (23) and the equivalent voltage vector $\mathbf{u}_{eq}$ (24) are the modified variables required by the pseudo-sliding mode control. Consequently, the switching condition (6) can be applied independently to each PEBB and the modulation algorithm works correctly, producing regular commutations and triangular modified flux errors $\boldsymbol{\lambda}$ with zero average value, similarly to Figure 5. Note that, however, quantities appearing in (24) are required to satisfy reasonable regularity assumptions, namely quantities i^* and u_m being suitable, Lipschitz-continuous functions with spectra limited to frequencies much lower than the switching frequency f_{sw}.

As mentioned, the considered system requires an effective management of the additional control degree of freedom to achieve consistent operation. In fact, the arbitrary variable u_m influences the duty cycle of each PEBB through the equivalent voltage $\mathbf{u}_{eq}$ (24).

The control variable u_m should be selected under two conditions: controllability and current minimization. Firstly, note that, with reference to Figure 3, the upper limit of

controllability condition (4) is represented, for each *i*-th port, by the port voltage v_i. Consequently, controllability condition is expressed, for each *i*-th PEBB as

$$0 < u_{eqi} < v_i,\ i \in [1, N] \tag{25}$$

Substituting the equivalent voltage expression (24) in (25) and recalling matrix **G** structure (21), the allowed range of u_m is obtained, for each *i*-th PEBB, from (25), resulting in

$$-\left(\mathbf{K}\mathbf{u}_{eq}'\right)_i \le u_m \le v_i - \left(\mathbf{K}\mathbf{u}_{eq}'\right)_i,\ i \in [1, N] \tag{26}$$

Note that the term $\mathbf{K}\mathbf{u}_{eq}'$ represents the voltage drop across each of the N switching inductors. The set (26) states the controllability limits as function of external voltages and derivatives of reference currents in (12). Secondly, consider that the fundamental purpose of the considered MC and, consequently, of each PEBB, is to transfer a given amount of power determined by the higher-level control. Therefore, in order to reduce the amplitude of the currents circulating through the inductors, it is wise to maximize $\mathbf{u}_{eq}$ according to (7). Consequently, u_m is conveniently selected according to

$$u_m = \min\left[\alpha v_i - \left(\mathbf{K}\mathbf{u}_{eq}'\right)_i\right],\ i \in [1, N] \tag{27}$$

with $\alpha<1$. Equation (27) defines u_m as the minimum of the external voltages, reduced of the voltage drop on the corresponding switching inductor. Furthermore, a precautionary term α is introduced to maintain a reasonable operative margin between the effective converter working condition and the upper controllability limit expressed in (26). Provided that a solution of (26) exists, selecting u_m by means of (27) ensures that condition (26) is respected for each PEBB, which is a necessary and sufficient condition for flux controllability, and by (12) for current controllability as well. The overall scheme representing the proposed control algorithm is reported in Figure 6.

As mentioned, a higher value of α is preferable since it allows to reduce the current necessary to transfer a given power (7), but it is necessary to understand the effect of α on the system dynamic performances. Considering dynamic issues, one should notice that it is not uncommon to temporarily violate (26): a typical example is a step-change in one current reference, which can be consequence, for example, of a load step-change. Because of the first of (12) and (23), the step-change is transferred to one or more flux errors **λ**. This step may imply a virtually infinite instantaneous derivative in (12) and consequently, condition

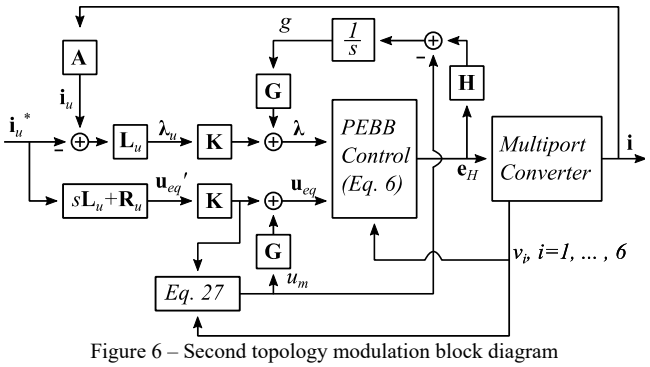

Figure 6 – Second topology modulation block diagram

(25) is not satisfied, leading to a temporary control loss. In this condition, once (25) is satisfied again, the flux reaches its reference in a finite time with a derivative given by (22). Consider now the single *i*-th PEBB corresponding to the minimum in (27), and take into account (24), (27). Recalling that the *i*-th switched voltage e_{Hi} has two possible instantaneous values, 0 and v_i, it follows that the positive and negative flux derivatives in (22) are, respectively, given by

$$\left(\frac{d\lambda_i}{dt}\right)_+ = v_i - u_{eq\,i} = (1-\alpha)v_i,\ \left(\frac{d\lambda_i}{dt}\right)_- = -u_{eq\,i} = -\alpha v_i \tag{28}$$

Clearly, a higher value of α implies a lower positive slope, and therefore a longer reaching phase in case of load increment and a shorter reaching phase in case of load reduction. Since it is not possible to assume a priori the sign of possible load step-changes, the maximum dynamic performances are obtained for α=0.5, which implies that positive and negative derivatives are the same. For clarity, the ideal local behaviour of the sliding variable λ with different values of α in presence of a step increase and decrease in reference current is reported in Figure 7. Considering system efficiency, it is useless to choose $\alpha < 0.5$, and consequently the useful range can be chosen as $0.5 \le \alpha < 1$; in this range controllability condition (26) is respected for reasonable transients. Note that the slower the expected transients are, the higher values of α should be selected in order to improve system efficiency; the faster the expected transients are, the smaller values of α should be selected in order to improve dynamic performances.

4.2. Considerations on System and Control Modularity

Some significant considerations regarding system modularity are hereby presented. In fact, in the previous Sections the control problem has been considered in general terms: in particular, $\mathbf{L}_u$ matrix non-singularity has been the only assumption regarding the inductance set, such that mutual couplings and different inductors for each PEBB are allowed. In fact, one could even consider to use N-1 inductors to reduce the converter cost, weight and volume. However, the considered MC can be easily realized by means of a totally modular structure from a hardware point of view, which introduces significant advantages in practical applications, such as increased flexibility and reduce repair time. Consequently, it is of interest to investigate in which terms and under which conditions also the control structure can be realized by means of a modular system.

In these regards, consider that, as long as the presented control applies to a general inductive network, it requires a

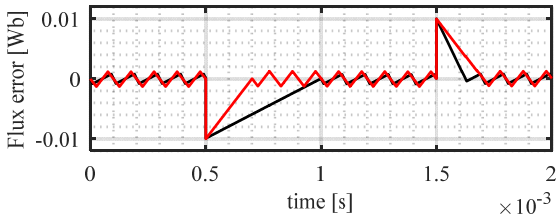

Figure 7 - Ideal local behaviour of the sliding function λ with $\alpha = 0.8$ (black) and $\alpha = 0.5$ (red) in case of: step increase in reference current (t = 0.5 *ms*), step decrease in reference current (t = 1.5 *ms*)

totally centralized architecture, in that the signal driving the switching of one PEBB (23) depends on all PEBB currents. On the contrary, when an inductive network consisting of N equal, star-connected inductances L (and, consequently, resistances R) (Figure 3), it stands

$$\mathbf{L} = L\mathbf{1}_N, \quad \mathbf{R} = R\mathbf{1}_N \tag{29}$$

Consequently, considering (10), (12), (21) and (29), it is easy to prove that (23) is composed by N independent terms, namely

$$\lambda_i = L\left(i_i - i_i{}^*\right) + g, \ i \in [1,N] \tag{30}$$

Hence, under the condition of equal inductances, (30) implies that the signal driving each PEBB depends only on its own PEBB current and on one common decoupling signal g, and not on other PEBBs currents; this allows designing a simpler and almost completely modular structure.

The case of N, equal, star-connected inductances introduces also a significant simplification in controllability condition. In fact, considering (29), it is easy to prove that (26) can be reformulated as

$$-\left(L\frac{di_i^*}{dt} + Ri_i^*\right) \le u_m \le v_i - \left(L\frac{di_i^*}{dt} + Ri_i^*\right), \ i \in [1, N] \tag{31}$$

Consequently, in case of N equal inductances and resistances, the upper and lower limits for the common voltage term u_m can be calculated, for each i-th port and instant by instant, depending only on the measured voltage v_i and reference current i_i^* of that port. On the contrary, in case of a general set of inductances, those limits would depend on a combination of all ports quantities (26). Considering now (31), it is possible to rearrange (27) as

$$u_m = \min\left[\alpha v_i - \left(L\frac{di_i^*}{dt} + Ri_i^*\right)\right], \ i \in [1, N] \tag{32}$$

with $\alpha<1$.

Consequently, in case of N, equal star connected switching inductors, a centralized controller is necessary to collect the required measures and to generate the signals g and u_m, while the remaining portions of the control of each port can be realized in a totally modular fashion. These considerations highlight that the proposed control can be successfully applied to the considered topology, resulting in a modular and substantially decoupled control structure.

5. Control Design for Application to LVDC Systems

The considered case study for application to LVDC systems comprises N=6 ports, as reported in Figure 8. For both topologies, port 1 is connected to a DC grid, which acts as an external power source. Port 2 is connected to supercapacitor (SC) banks, which allows maintaining high dynamic performances disregarding of grid dynamics, and port 3 is connected to batteries, realizing UPS functionality. Port 4 is connected to a PV source, which is treated as a load since it requires a predetermined voltage, obtained from an MPPT algorithm. Ports 5 and 6 are connected to loads.

The higher-level control is fully modular, in that all ports that are not used to interface controllable power sources use identical control structures and the centralized control is only needed to manage the different power sources. Switching inductances are selected equal for all ports: this implies a significant simplification in lower-level control for the second topology, according to discussion in Section 4.2. Anyway, the presented control allows to manage a general set of inductances. In the following, the control aspects common to both topologies are discussed in Section 5.1, while Sections 5.2 and 5.3 cover, respectively, the control aspects typical of the first and second topology.

5.1. Common Higher-level Control

The control design should firstly guarantee stable load voltages v_4, v_5, v_6 in all conditions (v_4 may be variable according to PV MPPT, not discussed in this paper). In order to get a single approach for both configurations, the control is firstly formulated in power variables. For the aforementioned ports, at capacitor terminals, it stays

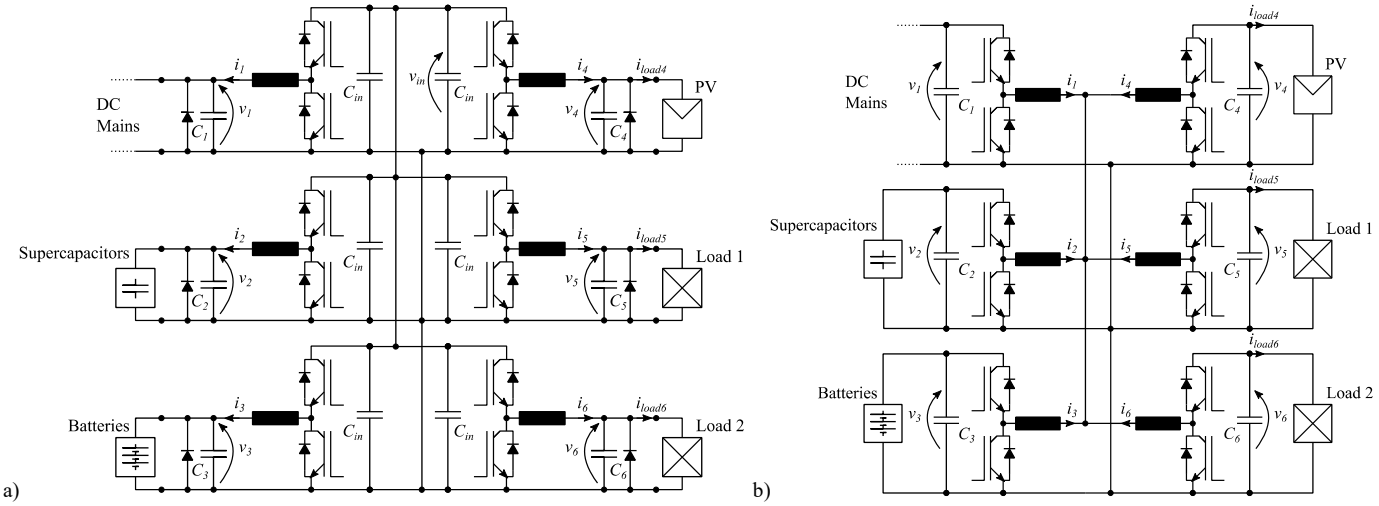

Figure 8 – Case study schematics: a) first topology and b) second topology

$$P_i = \frac{d}{dt}\left(\frac{1}{2}C_i v_i^2\right) + v_i \cdot i_{load\ i},\ i \in [4,6] \tag{33}$$

being $i_{load\ i}$ the current absorbed by the load connected to the *i*-th port. According to the inverse dynamic approach [48], let's define the dynamic voltage error equation

$$\left(v_i^* - v_i\right) + T_1 \cdot \frac{d}{dt}\left(v_i^* - v_i\right) + \frac{1}{T_2}\int\left(v_i^* - v_i\right)dt = 0,\ i \in [4,6] \tag{34}$$

where T_1, T_2 are constants to be assigned to obtain the desired damping and dynamic response. Note that, for this and the subsequent similar expressions, the value of T_1, T_2 is constrained only by the limited converter switching frequency. Considering (33), it follows

$$\frac{d}{dt}\left(v_i^* - v_i\right) = \frac{d}{dt}v_i^* + \frac{1}{C_i}\left(i_{load\ i} - \frac{P_i}{v_i}\right),\ i \in [4,6] \tag{35}$$

Substituting (35) in (34) and under the condition $P_i = P_i^*$, it is possible to obtain the port reference power for voltage regulation, which results in

$$P_i^* = v_i\left[C_i\frac{d}{dt}v_i^* + i_{load\,i} + g_{1i}\left(v_i^* - v_i\right) + g_{2i}\int\left(v_i^* - v_i\right)dt\right],\ i \in [4,6] \tag{36}$$

where $g_{1\,i} = C_i/T_1$, $g_{2\,i} = C_i/(T_1T_2)$. The reference current can be obtained from the reference power, but the expression depends on the specific topology; consequently, it will be reported in Section 5.2 and 5.3. The voltage control scheme resulting from (36) is reported in Figure 9.

Stated the control of v_4, v_5, v_6, it is necessary to determine power references for ports 1 to 3. Current references will be defined in Section 5.2 and 5.3. Let's define the global source reference power $P_g^* = P_1^* + P_2^* + P_3^*$, which represents the sum of the powers exchanged with the controllable power sources necessary to maintain the power balance. P_g^* must be split into ports 1 to 3 by means of a suitable logic, such as

$$\begin{cases} P_1^* = \beta_1 P_g^* \\ P_2^* = \beta_2 P_g^* \\ P_3^* = \beta_3 P_g^* \end{cases},\quad \sum_{i=1}^{3}\beta_i = 1 \tag{37}$$

Power sharing among different sources does not generally require further control loops, in that it consists of a unity-sum set of gains. In this paper, batteries are intended as UPS, such that port 3 will have a non-null reference current only when grid is out of service. On the contrary port 2, since intended as power-smoothing function, will have a non-null reference current only during transients. Nevertheless, it is possible to integrate in the MC control any storage management algorithm. For simplicity, only the faster dynamics are considered, while the slower dynamics, such as SCs and batteries State Of Charge (SOC) control, are neglected. A suitable strategy to obtain these results is the definition of rate-limiter functions to determine the reference power of each source in case of abrupt load changes or grid black-outs. However, these aspects, as well as the SOC control, are well established in literature [6] and hence lies outside the purpose of this paper.

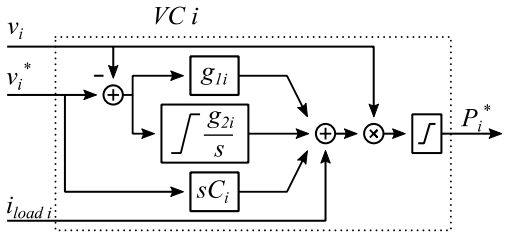

Figure 9 – Port voltage control (VC) block diagram for the *i*-th port

5.2. First Topology Higher-level Control

The internal DC bus voltage can be controlled considering the power balance at the internal DC bus. Neglecting power losses and energy stored in switching inductors, which are usually small and, however, are compensated by control integral terms in steady-state, this results in

$$P_g = \frac{d}{dt}\left[\frac{1}{2}\cdot 6C_{in}v_{in}^2\right] + \sum_{i=4}^{6} v_i \cdot i_i \tag{38}$$

where P_g is defined as the sum of the powers injected in the DC bus by power-controlled ports, namely $P_g = P_1 + P_2 + P_3$. By means of the same inverse dynamic approach reported in the previous paragraph, (38) leads to the control of the DC bus voltage through the source reference power:

$$P_g^* = v_{in}\left[6C_{in}\frac{d}{dt}v_{in}^* + g_{1\,in}\left(v_{in}^* - v_{in}\right) + g_{2\,in}\int\left(v_{in}^* - v_{in}\right)dt\right] + \sum_{i=4}^{6} P_i^* \tag{39}$$

where $g_{1\,in} = 6C_{in}/T_{P1}$, $g_{2\,in} = 6C_{in}/(T_{P1}T_{P2})$. T_{P1}, T_{P2} are constants to be assigned to obtain the desired damping and dynamic response. Power (39) allows assigning (37). Being now the reference power defined for each port by means of (36), (37), current references are obtained as

$$i_i^* = -\frac{P_i^*}{v_i} \quad i \in [1,3],\quad i_i^* = \frac{P_i^*}{v_i} \quad i \in [4,6] \tag{40}$$

References (40) are applied to PEBB control presented in Section 3. The resulting higher-level control scheme for the first MC topology is reported in Figure 10. Each current reference magnitude should also be limited to a predetermined value, depending on the semiconductors maximum current, in order to avoid possible issues in case of external faults. This can also have a significant role in system protection design [9].

5.3. Second Topology Higher-level Control

The procedure described in Section 4 is applied with N=6. Neglecting power losses and energy stored in switching inductors, the global reference power P_g^* is then obtained as

$$P_g^* = \sum_{i=4}^{6} P_i^* \tag{41}$$

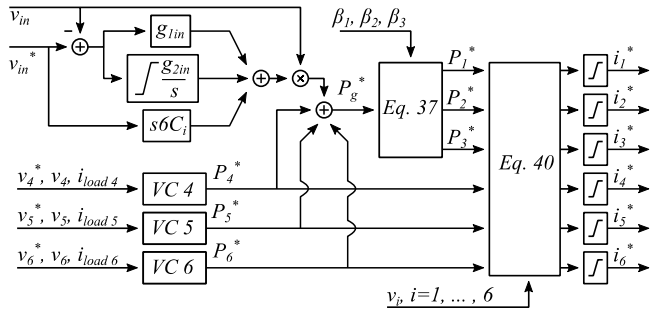

Figure 10 – First topology control block diagram

Being the reference power defined at each port, PEBB current references are obtained considering the power balance in the internal bus. In these regards, consider that each PEBB power is expressed as (7). Since powers in *L*, *R* parameters are neglected, recalling (12), (24), this results in

$$i_i^* = \frac{P_i^*}{u_m}, \quad i \in [1,3], \quad i_i^* = -\frac{P_i^*}{u_m}, \quad i \in [4,6] \tag{42}$$

The resulting higher-level control scheme for the second MC topology is reported in Figure 11. Note that, according to the control algorithm developed in Section 4.2, the six module currents are treated as independent for modularity reasons and to exploit the robustness and dynamic properties of sliding mode controllers. In fact, power balance (37), (41) implies that the sum of the six references (42) is null. Again, each current reference magnitude should also be limited to a predetermined value, depending on the semiconductors maximum current, to avoid possible issues in case of faults.

6. Dynamic Modeling and Stability Analysis

The issues of dynamic modelling and stability are here addressed considering the two-layer structure of the proposed control. Firstly, some considerations on current control stability are presented. State-space models are then derived for the system in sliding condition.

6.1. Pseudo-sliding Mode Current Control

The stability properties of sliding mode controllers are well-known in literature [38] - [46]. For this application, it is worth noting that the requirement which allows reaching sliding condition in finite time and maintaining sliding condition thereafter is expressed by (4) for the first topology and by (26) for the second topology. Those conditions are usually satisfied for a correctly designed system under non-restrictive hypothesis, which in this case can be reduced to v_i^* and $i_{load\,i}$ being suitable limited, Lipschitz-continuous functions. While this is granted for v_i^*, two significant exceptions must be mentioned for $i_{load\,i}$, namely line fault and load step-change. However, in these cases, it is usually possible to approximate $i_{load\,i}$ by means of a Lipschitz-continuous function except from a limited step-change. Consequently, (4) and (26) are satisfied for any time except the instant corresponding to the step-change and, under these assumptions, sliding condition is lost at the instant corresponding to the step-change, but then reached again in finite time, according to discussion reported in Section 4.1. A general example of this kind of response to perturbations is

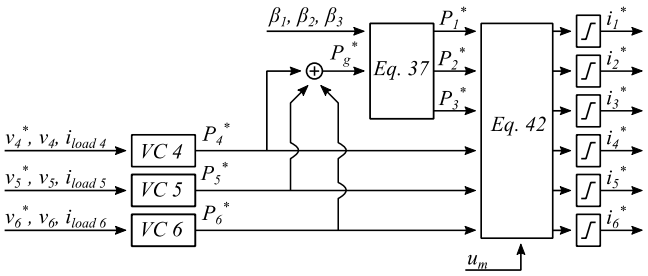

Figure 11 – Second topology control block diagram

depicted in Figure 7 in terms of flux errors, while more specific examples will be presented for each topology in Section 8.

6.2. First Topology

With reference to Figure 8 a, assume the system to be in sliding condition ($i_i = i_i^*$, which implies $P_i = P_i^*$). The currents i_i are considered the system control variables being imposed by the pseudo-sliding-mode controller, such that, in sliding condition, each PEBB can be modelled as a controlled ideal current source. The states to be included in the dynamic model are the capacitor voltages v_i and the internal bus voltage v_{in}, which are also the controlled variables. Considering (38), (33), (40), system states and control variables can be related considering the following equations:

$$\begin{cases} \dfrac{d}{dt} v_{in} = \dfrac{1}{6C_{in}} \left(\dfrac{P_g}{v_{in}} - \sum_{i=4}^{6} \dfrac{v_i i_i}{v_{in}} \right) \\ \dfrac{d}{dt} v_i = \dfrac{1}{C_i} \left(i_i - i_{load\,i} \right), \; i \in [4,6] \end{cases} \tag{43}$$

The resulting state-space model can be formulated as

$$\begin{cases} \dot{\mathbf{x}}' = \mathbf{A}'\mathbf{x}' + \mathbf{B}'\mathbf{u}' + \mathbf{M}'\mathbf{d}' \\ \mathbf{y}' = \mathbf{x}' \end{cases} \tag{44}$$

where

$$\mathbf{x}' = \begin{bmatrix} v_{in} \\ v_4 \\ v_5 \\ v_6 \end{bmatrix}, \; \mathbf{u}' = \begin{bmatrix} P_g \\ i_4 \\ i_5 \\ i_6 \end{bmatrix}, \; \mathbf{d}' = \begin{bmatrix} i_{load\,4} \\ i_{load\,5} \\ i_{load\,6} \end{bmatrix} \tag{45}$$

A' is a null 4x4 matrix, which is consistent considering that, in sliding condition, the converter output voltages are naturally decoupled. **B'** is a 4x4 matrix defined as

$$\mathbf{B}' = \begin{bmatrix} \dfrac{1}{v_{in} \cdot 6C_{in}} & -\dfrac{v_4}{v_{in} \cdot 6C_{in}} & -\dfrac{v_5}{v_{in} \cdot 6C_{in}} & -\dfrac{v_6}{v_{in} \cdot 6C_{in}} \\ & 1/C_4 & & \\ & & 1/C_5 & \\ & & & 1/C_6 \end{bmatrix} \tag{46}$$

and **M'** is a 4x3 matrix defined as

$$\mathbf{M}' = \begin{bmatrix} 0 & 0 & 0 \\ -1/C_4 & & \\ & -1/C_5 & \\ & & -1/C_6 \end{bmatrix} \tag{47}$$

Note that, as usual for power converters, the system is intrinsically non-linear (**B***'* is a function of the states **x**'), which is consistent with the fact that power converters conserve instantaneous power.

In order to evaluate the stability properties of the controlled system, the control laws are now introduced in system modeling. To take care of the integral terms, as usual in linear systems analysis, let's define an auxiliary state **w**' such that

$$\dot{\mathbf{w}}' = \mathbf{x}'^{*} - \mathbf{x}' \tag{48}$$

The controls laws are assigned by means of (36), (39), (40). For stability considerations, it is common to impose null references ($\mathbf{x}'^{*} = 0$) for simplicity, since the system stability properties do not depend on system inputs. Under this assumption, it is possible to write the system control variables in matrix form as

$$\mathbf{u}' = \mathbf{G}_1'\mathbf{x}' + \mathbf{G}_2'\mathbf{w}' + \mathbf{P}'\mathbf{d}' \tag{49}$$

where

$$\mathbf{G}_1' = \begin{bmatrix} -g_{1in}v_{in} & -g_{14}v_4 & -g_{15}v_5 & -g_{16}v_6 \\ & -g_{14} & & \\ & & -g_{15} & \\ & & & -g_{16} \end{bmatrix}$$

$$\mathbf{G}_2' = \begin{bmatrix} g_{2in}v_{in} & g_{24}v_4 & g_{25}v_5 & g_{26}v_6 \\ & g_{24} & & \\ & & g_{25} & \\ & & & g_{26} \end{bmatrix}, \quad \mathbf{P}' = \begin{bmatrix} v_4 & v_5 & v_6 \\ 1 & & \\ & 1 & \\ & & 1 \end{bmatrix} \tag{50}$$

Considering (44) - (47), (48), and substituting (49), (50) in (44), the augmented dynamic system results in

$$\begin{cases} \dot{\mathbf{x}}' = \mathbf{B}'\mathbf{G}_1'\mathbf{x}' + \mathbf{B}'\mathbf{G}_2'\mathbf{w}' + \left(\mathbf{B}'\mathbf{P}' + \mathbf{M}'\right)\mathbf{d}' \\ \dot{\mathbf{w}}' = -\mathbf{x}' \\ \mathbf{y}' = \mathbf{x}' \end{cases} \tag{51}$$

Observing that **B**'**P**'+**M**' = **0**, the augmented dynamic system can be reformulated as

$$\begin{cases} \begin{bmatrix} \dot{\mathbf{x}}' \\ \dot{\mathbf{w}}' \end{bmatrix} = \tilde{\mathbf{A}}' \begin{bmatrix} \mathbf{x}' \\ \mathbf{w}' \end{bmatrix} \\ \mathbf{y}' = \mathbf{x}' \end{cases} \tag{52}$$

The augmented dynamic matrix $\tilde{\mathbf{A}}'$ is then obtained as

$$\tilde{\mathbf{A}}' = \begin{bmatrix} \mathbf{T}_1'_{4x4} & \mathbf{T}_2'_{4x4} \\ -\mathbf{1}_4 & \mathbf{0}_4 \end{bmatrix} \tag{53}$$

with $\mathbf{1}_4$ and $\mathbf{0}_4$ representing, respectively, a unity and a null 4×4 matrix and

$$\begin{aligned} \mathbf{T}_1' &= \mathbf{B}'\mathbf{G}_1' = -diag\left[\frac{1}{T_{P1}}, \frac{1}{T_1}, \frac{1}{T_1}, \frac{1}{T_1}\right] \\ \mathbf{T}_2' &= \mathbf{B}'\mathbf{G}_2' = diag\left[\frac{1}{T_{P1}T_{P2}}, \frac{1}{T_1T_2}, \frac{1}{T_1T_2}, \frac{1}{T_1T_2}\right] \end{aligned} \tag{54}$$

Note that, while the original system is non-linear (**B***'* (46) is a function of the states **x**'), the controlled system in sliding condition is linear due to the inverse dynamic control design.

The characteristic polynomial of $\tilde{\mathbf{A}}'$ results in

$$\det(s\mathbf{I}_8 - \tilde{\mathbf{A}}') = \left(s^2 + \frac{s}{T_{P1}} + \frac{1}{T_{P1}T_{P2}}\right)\left(s^2 + \frac{s}{T_1} + \frac{1}{T_1T_2}\right)^3 \tag{55}$$

The roots of the characteristic polynomial have negative real part as long as parameters T_{P1}, T_{P2}, T_1, T_2 are positive, which is granted with the adopted tuning method, and hence the controlled system is asymptotically stable and the eigenvalues of the dynamic matrix are arbitrarily assigned. These results are obtained considering the system in sliding condition. When sliding condition is momentarily lost, as discussed in Section 6.1, during the subsequent reaching phase an error on voltage is cumulated. When sliding condition is restored, the residual error is forced to zero with the dynamic assigned by (55).

6.3. Second Topolgy

With reference to Figure 8 b, assume the system to be in sliding condition. Under the same assumptions introduced for the first topology analysis, the states to be included in the dynamic model are the capacitor voltages v_i, which are also the controlled variables. Considering (33), (42), system states and control variables can be related considering the following equations:

$$\frac{d}{dt}v_i = -\frac{1}{C_i}\left(\frac{u_m}{v_i}i_i + i_{load\ i}\right), \quad i = [4,6] \tag{56}$$

The resulting state-space model can be formulated as

$$\begin{cases} \dot{\mathbf{x}}'' = \mathbf{A}''\mathbf{x}'' + \mathbf{B}''\mathbf{u}'' + \mathbf{M}''\mathbf{d}'' \\ \mathbf{y}'' = \mathbf{x}'' \end{cases} \tag{57}$$

where

$$\mathbf{x}'' = \begin{bmatrix} v_4 \\ v_5 \\ v_6 \end{bmatrix}, \quad \mathbf{u}'' = \begin{bmatrix} i_4 \\ i_5 \\ i_6 \end{bmatrix}, \quad \mathbf{d}'' = \begin{bmatrix} i_{load\ 4} \\ i_{load\ 5} \\ i_{load\ 6} \end{bmatrix} \tag{58}$$

A'' is a null 3x3 matrix, **B**'' is a 3x3 matrix defined as

$$\mathbf{B}'' = -diag\left[\frac{u_m}{v_4C_4}, \frac{u_m}{v_5C_5}, \frac{u_m}{v_6C_6}\right] \tag{59}$$

and **M**'' is a 3x3 matrix defined as

$$\mathbf{M}'' = -diag\left[\frac{1}{C_4}, \frac{1}{C_5}, \frac{1}{C_6}\right] \tag{60}$$

In order to evaluate the controlled system stability properties, the control laws are now introduced in system modelling. To take care of the integral terms, let's define an auxiliary state **w**" such that

$$\dot{\mathbf{w}}'' = \mathbf{x}''^* - \mathbf{x}'' \tag{61}$$

The control laws are assigned by means of (36), (42). Exploiting the auxiliary state (61) and applying the same procedure and hypothesis considered for the first topology, including null references, the system control variables can be written in matrix form as

$$\mathbf{u}'' = \mathbf{G}_1''\mathbf{x}'' + \mathbf{G}_2''\mathbf{w}'' + \mathbf{P}''\mathbf{d}'' \tag{62}$$

where

$$\begin{aligned}
\mathbf{G}_1'' &= diag\left[\frac{g_{14}v_4}{u_m}, \frac{g_{15}v_5}{u_m}, \frac{g_{16}v_6}{u_m}\right] \\
\mathbf{G}_2'' &= -diag\left[\frac{g_{24}v_4}{u_m}, \frac{g_{25}v_5}{u_m}, \frac{g_{26}v_6}{u_m}\right] \\
\mathbf{P}'' &= -diag\left[\frac{v_4}{u_m}, \frac{v_5}{u_m}, \frac{v_6}{u_m}\right]
\end{aligned} \tag{63}$$

Considering (57) - (60), (61), and substituting (62), (63) in (57), the augmented dynamic system results in

$$\begin{cases}
\dot{\mathbf{x}}'' = \mathbf{B}''\mathbf{G}_1''\mathbf{x}'' + \mathbf{B}''\mathbf{G}_2''\mathbf{w}'' + \left(\mathbf{B}''\mathbf{P}'' + \mathbf{M}''\right)\mathbf{d}'' \\
\dot{\mathbf{w}}'' = -\mathbf{x}'' \\
\mathbf{y}'' = \mathbf{x}''
\end{cases} \tag{64}$$

Observing that **B**"**P**"+**M**" = **0**, the augmented dynamic system can be reformulated as

$$\begin{cases}
\begin{bmatrix}\dot{\mathbf{x}}'' \\ \dot{\mathbf{w}}''\end{bmatrix} = \tilde{\mathbf{A}}''\begin{bmatrix}\mathbf{x}'' \\ \mathbf{w}''\end{bmatrix} \\
\mathbf{y}'' = \mathbf{x}''
\end{cases} \tag{65}$$

The augmented dynamic matrix $\tilde{\mathbf{A}}''$ is defined as

$$\tilde{\mathbf{A}}'' = \begin{bmatrix}\mathbf{T}_{1\,3x3}'' & \mathbf{T}_{2\,3x3}'' \\ -\mathbf{1}_3 & \mathbf{0}_3\end{bmatrix} \tag{66}$$

with

$$\mathbf{T}_1'' = \mathbf{B}''\mathbf{G}_1'' = -\frac{1}{T_1}\mathbf{1}_3, \quad \mathbf{T}_2'' = \mathbf{B}''\mathbf{G}_2'' = \frac{1}{T_1T_2}\mathbf{1}_3 \tag{67}$$

Note that, also in this case, while the original system is non-linear (**B**" (59) is a function of the states **x**"), the controlled system in sliding condition is linear due to the inverse dynamic control design.

The characteristic polynomial of $\tilde{\mathbf{A}}''$ results in

$$\det(s\mathbf{I}_6 - \tilde{\mathbf{A}}'') = \left(s^2 + \frac{s}{T_1} + \frac{1}{T_1T_2}\right)^3 \tag{68}$$

The considerations reported in the previous paragraph still apply.

7. Fault Analysis

7.1. First Topology

In the first topology, controllability condition is expressed by (4). A pole-to-pole fault on the internal DC-bus causes the internal voltage to fall to zero; since external voltages are initially non-null, (4) is violated and uncontrolled currents flow through free-wheeling diodes in all PEBBs, and hence some of them may be damaged during the fault. On the contrary, a pole-to-pole fault on one port does not interfere with (4). Outputs currents are always kept under control, such that no faults on one output port can affect other ports or the internal DC-bus.

Under fault condition, the control can limit the fault current to a predetermined, bearable value, such that the converter is self-protected during faults: the current is kept equal to its maximum value until the fault is resolved and voltage can be recovered. If the fault is not resolved in a predetermined time (reasonably, few seconds) the current reference is set to zero for safety reasons.

7.2. Second Topology

In the second topology, controllability condition is expressed by (25), (26). In case of a pole-to-pole fault on the internal DC-bus, power transfer capability (7) is lost for the whole system, but (25) is respected and each PEBB current can be kept under control. Therefore, I/O powers fall to zero but none of the PEBBs is damaged by the fault. This allows automatic restart and regular operation after the fault is eliminated. On the contrary, in case of a pole-to-pole fault on one port, power transfer capability (7) is again lost for the whole system and (25) is violated for the faulted port only, while it is still respected for the other ports. This implies that no uncontrolled currents can circulate since healthy ports can still control their currents. Therefore, no PEBBs can suffer damages from pole-to-pole faults. Summarizing, in this configuration no pole-to-pole fault can cause damage in any PEBB; a pole-to-pole fault on a port or on the internal DC-bus causes the converter to stop its operation until the fault is removed.

Under fault condition, the control can limit the fault current to a predetermined, bearable value, but the faulted port is no more controllable. This suggests a possible strategy to limit the impact of external faults: once the fault is detected, all reference currents are set to zero and all valves are opened. This procedure rapidly forces all currents in the DC link to zero, such that a mechanical switching device can isolate the faulted port with no need to open a significant current. Once the faulted port is removed, the MC can be restarted: this procedure does not impede the loads connected to healthy ports to suffer from voltage dips but allows a fast restoration of correct operating conditions.

8. Simulation Results

Simulations have been performed to substantiate the considerations presented on both topologies and related controls. Three events have been considered in order to show the control effectiveness in managing abrupt load variations, main grid failure and external faults. Details are reported in Table 1. Loads and sources parameters are reported in Table 2. Converter and control parameters for the first and second topology are reported, respectively, in Table 3 and Table 4. All simulations have been performed in MATLAB/Simulink environment using standard Simscape component models.

8.1. First Topology

Firstly, the load step change is considered: port 5 voltage v_5 and current i_5 are reported in Figure 12 and Figure 13, respectively. One can notice that the transient exhibits the expected behaviour. Initially, the load step-change causes a faster change in current reference, which, because of the time-derivative (3), causes a violation of controllability condition (4) and consequent loss of sliding condition. This fact is highlighted by the short-term disjunction between the measured current and its reference in Figure 13. After that, condition (4) is satisfied again and reaching phase is established. Sliding condition is hence reached in a finite time. During the above two phases, voltage is subject to an unavoidable perturbation. Once sliding condition is reached, voltage error is forced to zero following the dynamic set by (34), such that reference voltage is restored in about 25 *ms* (≅ 5 time constants).

Secondly, the main grid failure is considered: the power absorbed from the available sources is reported in Figure 14, while the internal bus voltage is reported in Figure 15 and port 5 voltage during the transition is reported in Figure 16. One can notice that SCs and batteries correctly cooperate to provide the

Table 1 – Simulation Events

Time [s]	*Affected Port*	*Event*
0.1	*5*	*Load step-change from 20 kW to 40 kW*
0.2 – 0.5	*1*	*Main grid out of service*
0.9	*6*	*External fault (short circuit, fault impedance: R = 100 mΩ, L = 10 μH)*

Table 2 – Loads and Sources

Port	*Connection*	*Details*
1	*Main DC Grid*	*400 V, limited dynamics*
2	*SCs*	*48 V, 165 F per module; 9 series connected modules*
3	*Batteries*	*12 V, 100 Ah per module; 35 series connected modules*
4	*PV panels*	*75 kW, no-load voltage 450 V (assumed constant 50 kW in simulation)*
5	*Load 1*	*400 V, 50 kW, resistive load*
6	*Load 2*	*400 V, 50 kW, resistive load*

Table 3 – First MC Parameters

Rated Values		*Components*		*Control*	
Parameter	*Value*	*Par.*	*Value*	*Par.*	*Value*
Internal Voltage	*500 V*	L_i	*1 mH*	T_1	*5 ms*
		R_i	*10 mΩ*	T_2	*5 ms*
Switching Frequency	*10 kHz*	C_i	*6.8 mF*	T_{P1}	*5 ms*
Maximum PEBB Current	*250 A*	C_{in}	*1.1 mF*	T_{P2}	*5 ms*

Table 4 – Second MC Parameters

Rated Values		*Components*		*Control*	
Parameter	*Value*	*Par.*	*Value*	*Par.*	*Value*
Internal Voltage	*-*	L_i	*0.1 mH*	T_1	*5 ms*
Switching Frequency	*10 kHz*	R_i	*10 mΩ*	T_2	*5 ms*
Maximum PEBB Current	*500 A*	C_i	*4 x 6.8 mF*	α	*0.8*

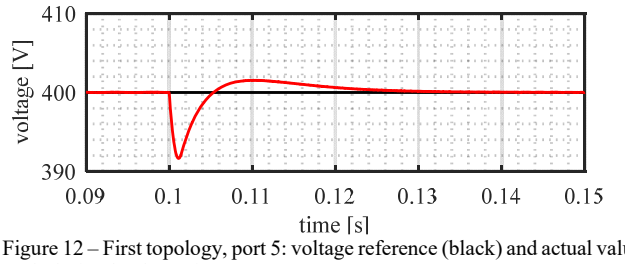

Figure 12 – First topology, port 5: voltage reference (black) and actual value (red) during load transient

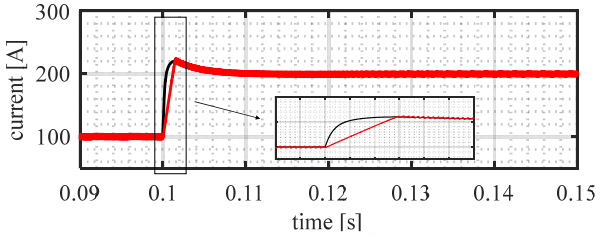

Figure 13 – First topology, port 5: current reference (black) and actual value (red) during load transient

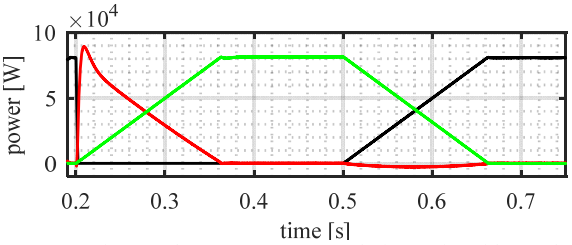

Figure 14 – First topology, sources power during main grid out of service and reconnection: main grid (black), SCs (red) and batteries (green).

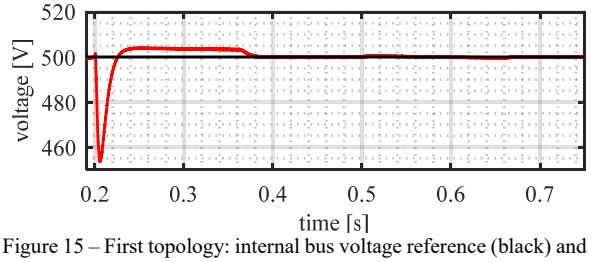

Figure 15 – First topology: internal bus voltage reference (black) and actual value (red) during main grid out of service and reconnection.

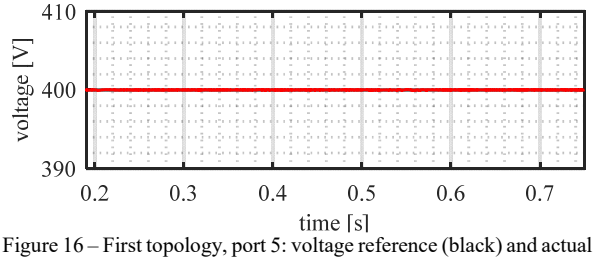

Figure 16 – First topology, port 5: voltage reference (black) and actual value (red) during main grid out of service and reconnection

power requested from the loads, according to (37), while load voltages are unaffected by the main grid outage. This is consistent with the considerations reported in Sections 6.1, 6.2: only the module connected to the grid loses sliding condition due to the fault, so the only voltage which should be affected by any disturbance is the internal voltage, since it is controlled by that module. As expected, the SCs are heavily involved in the disconnection from the grid, which is an unexpected transient, while they are less involved in grid reconnection, since it is a controlled transient. The internal voltage is strictly controlled too, with a perturbation during the disconnection from the grid, which, anyway, does not impact on load voltages, and a negligible one during the reconnection: this is consistent with the fact that the grid disconnection, being an unexpected, uncontrolled transient, causes a loss of sliding condition on port 1 and requires a fast intervention of the SCs to limit internal voltage deviation. On the contrary, the reconnection to the grid is a controlled transient, such that all ports maintain sliding condition and only a negligible perturbation on internal voltage is recognized.

Finally, the short circuit on port 6 is considered: port 6 voltage v_6 and current $i_{load\ 6}$ are reported in Figure 17, while current i_6 is reported in Figure 18; port 5 voltage during the fault is reported in Figure 19. One can notice that, even though an uncontrolled fault current is experienced from the line/load, the current supplied by the converter remains controlled during the whole fault and is correctly limited to a predetermined value. Furthermore, the remaining port voltages are unaffected by the fault: this is again consistent with Section 6.2, in that there is no reason for those ports to lose sliding condition.

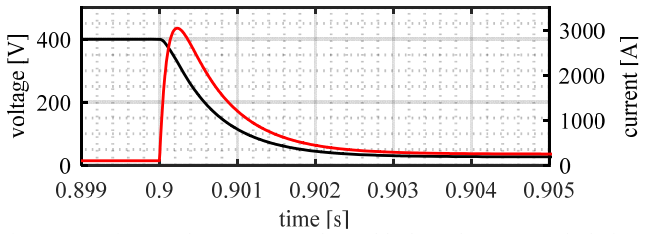

Figure 17 – First topology, port 6: voltage (black) and current (red) during the short circuit on port 6

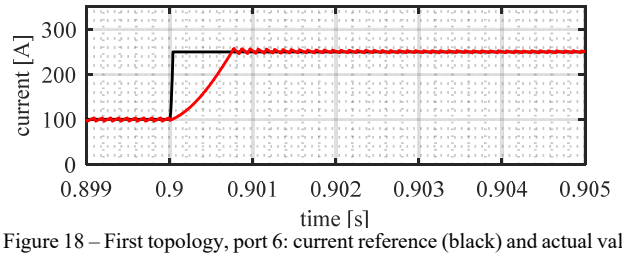

Figure 18 – First topology, port 6: current reference (black) and actual value (red) during the short circuit on port 6

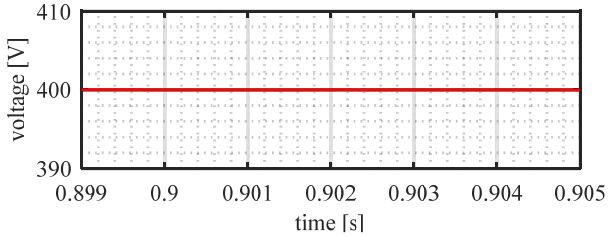

Figure 19 – First topology, port 5: voltage reference (black) and actual value (red) during the short circuit on port 6

8.2. *Second Topology*

Firstly, the load step change is considered: port 5 voltage v_5 and current i_5 are reported in Figure 20 and Figure 21, respectively. Analogously to the previous case, the transient exhibits the expected behaviour, except that the reaching phase is much shorter due to the smaller inductances used in this case, which allows for faster internal dynamics. Voltage is subject to an unavoidable perturbation due to the step change, but, once sliding condition is reached, voltage error is forced to zero following the dynamic set by (34), such that nominal voltage is restored in about 25 *ms* (≅ 5 time constants). Note also that the maximum voltage error is smaller in this case due to the faster reaching phase. Since the external capacitors are subject to a square-wave current ripple (with respect to triangular ripple in the first configuration), larger capacitors are required but still the external voltage is affected by a larger voltage ripple. The larger capacitors also contribute in reducing voltage dips depth.

Secondly, the main grid failure is considered: the power absorbed from the available sources is reported in Figure 22, the common voltage term u_m is reported in Figure 23 while port 5 voltage during the transition is reported in Figure 24. The considerations presented for the first topology are still valid, but the lack of the internal capacitors, which act as energy buffers, leads to an unavoidable, even though very small, perturbation on load voltages. In fact, for both the first and second topology, the fault on the main DC grid implies a loss of sliding condition on port 1. However, in the first topology the ports feeding loads can get the required energy from the internal bus capacitors during the short transitional period required to switch from the main grid to storage devices. This creates a larger perturbation on the internal bus, which does not affect any load and allows maintain constant load voltage. On the contrary, in the second topology the internal bus has no reactive elements except from switching inductances, such that the perturbation introduced by the loss of sliding condition on port 1 cannot be instantaneously

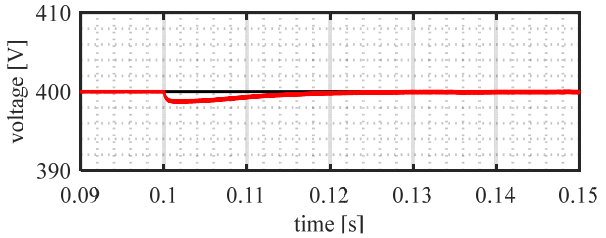

Figure 20 – Second topology, port 5: voltage reference (black) and actual value (red) during load transient

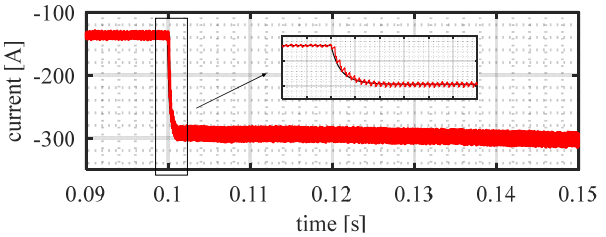

Figure 21 – Second topology, port 5: current reference (black) and actual value (red) during load transient

compensated draining energy from the internal bus capacitors. Consequently, the small error accumulated during the reaching phase of port 1 is forced to zero with the usual dynamic assigned by means of (34), resulting in the light perturbation depicted in Figure 24. Another significant difference regards the action necessary to correctly manage grid faults: while the first topology does not suffer from null external voltages, the second one cannot maintain correct operation with null external voltages. Consequently, in order to obtain correct operation when the grid is affected by a fault, it is necessary to isolate the MC port connected to the grid. Lastly, it is of interest to consider the common voltage term u_m profile: in fact, for the same reasons reported in Section 8.1 for the internal voltage bus of the first MC topology, it can be subject to major perturbation in case of power supply failure. However, it can be observed that u_m remains in a reasonable range (250 V - 300 V). Furthermore, a precise relation between the profile of u_m, defined from (27), and the source voltages can be noticed: when the grid goes out of service, the converter control switches the power supply from the grid to storage devices. The voltage on port 1 is no more significant from here on, since in case of grid faults the corresponding port is isolated. As programmed, supercapacitors are involved during fast transitions, while batteries are used for longer time scales due to their limited dynamics. Consequently, since both supercapacitors and batteries are initially charged to 400 V, in the instants immediately before the grid fault, the minimum in (27) is represented by the main grid port, while, after the grid fault, the port connected to supercapacitors represents the minimum in (27) and hence drives the value of u_m.

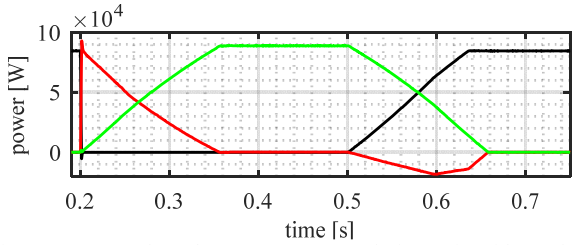

Figure 22 – Second topology, sources power during main grid out of service and reconnection: main grid (black), SCs (red) and batteries (green)

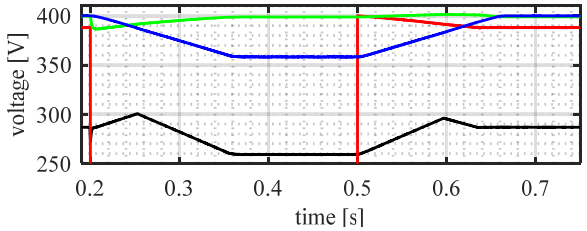

Figure 23 – Second topology: common voltage term um (black) and port voltages v1 (red), v2 (green) and v3 (blue) during main grid out of service and reconnection.

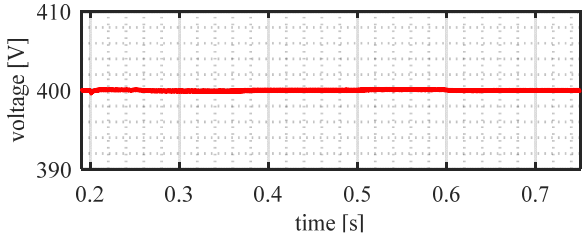

Figure 24 – Second topology, port 5: voltage reference (black) and actual value (red) during main grid out of service and reconnection

Indeed, it can be observed that, after the fault, the value of u_m rises since, as the power drained from supercapacitors decreases, the voltage drops on their internal resistance decreases. Successively, when batteries are providing more power than supercapacitors, their connection port becomes the minimum identified by (27), hence imposing the profile of u_m during the time range from roughly 0.35 s to 0.5 s. In fact, it can be observed that the higher the power drained from the batteries is, the lower the value of u_m. After 0.5 s, the power supply transition from storage devices to the main grid takes place, similarly to the aforementioned transition from grid to storage devices. The batteries port voltage still drives u_m up to roughly 0.6 s, where the main grid port represents again the minimum in (27).

Finally, the short circuit on port 6 is considered: port 6 voltage v_6 and current $i_{load\,6}$ are reported in Figure 25, while the current in port 6 switching inductance is reported in Figure 26. As expected, an uncontrolled fault current is experienced from the line/load. Considering the discussion on external fault reported in Section 7.2 and (26), it is clear that during the fault both sliding and reaching conditions are not respected on the faulted port; in addition, power transmission capability (7) is lost for the whole system. Anyway, sliding condition is maintained for the other ports: this allows to rapidly stop the system by setting all current references to zero, which also forces to zero the uncontrolled current flowing to the faulted port switching inductance. The faulted port is then mechanically isolated from the system, which can be restarted. Assuming reasonable times to detect the fault and isolate the faulted port (2.5 *ms* and 5 *ms*, respectively), the resulting port 5 voltage is reported in Figure

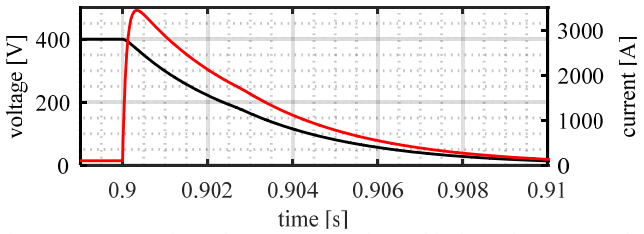

Figure 25 – Second topology, port 6: voltage (black) and current (red) during the short circuit on port 6

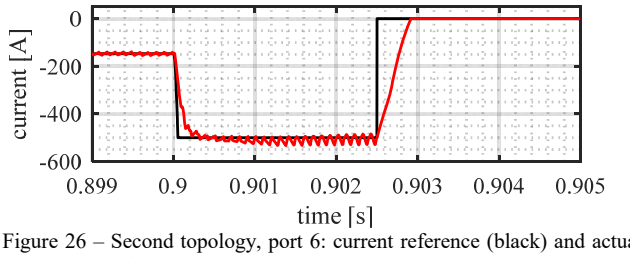

Figure 26 – Second topology, port 6: current reference (black) and actual value (red) in the switching inductance during the short circuit on port 6

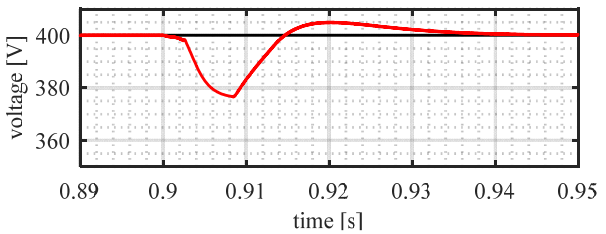

Figure 27 – Second topology, port 5: voltage reference (black) and actual value (red) during the short circuit on port 6

27. As expected, since the fault elimination procedure requires to set all reference currents to zero for a short time, a perturbation is recognized on healthy ports voltages. However, even if this perturbation is unavoidable, this proves that the limit of this second topology regarding external faults can be largely reduced by means of a suitable centralized control approach, which takes advantage from the MC structure.

9. Multiport Converters Comparison

The two considered topologies are both obtained by means of N PEBBs. The sizing of the first topology is similar to standard DC-DC converters. Considering equal external voltages, powers and switching frequency, the first topology requires, for an N port converter, N inductors and 2N capacitors; the second one requires N inductors and N capacitors. In the second configuration the inductors should withstand a higher current; on the other hand, the current ripple is determined by the difference among the duty cycles, which are usually homogeneous among all PEBBs, such that the internal inductances can be smaller in value. Conversely, port capacitors are subjected to a larger, square-waved ripple, which requires to use larger capacitors to match the desired voltage quality requirements. Overall, the second topology needs much smaller inductances and fewer but larger capacitors. Another significant difference between the two topologies is the usable voltage range: in the first topology, external voltages can be set at any positive value lower than the common internal voltage. On the contrary, in the second topology the external voltages can be theoretically set to any value higher than a common lower limit (27), while the higher limit is only related to technological issues. Finally, another difference is represented by the possibility of direct AC interface: it is easy to modify the first topology such that two or three PEBBs are used to realize a Front-end Converter (FEC), while, in the second configuration, AC interface requires a FEC cascaded to one port. Considering the different properties of the two topologies, both should be considered in a general-purpose approach.

Further differences emerge when the whole system, including controllers, is considered. Firstly, one should notice that, according to theoretical discussion reported in Sections 6 and 7, as long as the simulation results presented in Section 8, the two MCs are perfectly equivalent as long as sliding condition is maintained for all PEBBs. Then, it is possible to observe that slight differences appear when sliding condition is lost due to load step-change or grid black-out, mostly due to the different sizing of reactive elements leading to significantly different reaching times. Substantial differences appear when faults are considered: the first MC topology is robust with respect to external faults, including power supply failure/perturbations, but is prone to damages in case of faults on the internal bus. On the contrary, the second MC topology is prone to momentary loss of power transfer capability in case of external or internal faults, but it is resistant to possible semiconductor damages caused by those faults; simulation results have shown that it is possible to strongly mitigate the impact of external faults on voltage quality by means of suitable control strategies.

10. Conclusion

In this paper two MC topologies have been analyzed: control strategies, dynamic modeling, stability and fault behavior has been discussed for both topologies. Simulation results have been presented to substantiate the proposed control effectiveness both under regular and fault conditions. The comparison among the two considered topologies shows that both exhibits advantages and disadvantages.

The presented considerations suggest that the first topology is particularly interesting for centralized architectures where it is possible to have a protected internal DC bus. In this case the probability of internal faults becomes very low and hence it is possible to take advantage from the external fault insensitivity of the first MC topology. On the contrary, the second MC topology is particularly interesting for centralized architectures, where it is not possible to have a segregated internal bus, or for decentralized architectures with a distributed internal bus. Since in these cases it is not possible to significantly reduce the internal fault probability, it is wise to consider the second topology: in fact, while the first MC topology can be prone to damage in case of internal faults, it has been shown that the second one is robust with respect to internal faults and allows fast restart after fault elimination.

References

[1] F. Blaabjerg, Zhe Chen and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1184-1194, Sept. 2004.

[2] J. M. Carrasco et al., "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1002-1016, June 2006.

[3] M. E. Baran and N. R. Mahajan, "DC distribution for industrial systems: opportunities and challenges," in *IEEE Transactions on Industry Applications*, vol. 39, no. 6, pp. 1596-1601, Nov.-Dec. 2003.

[4] M. Kumar, S. C. Srivastava and S. N. Singh, "Control Strategies of a DC Microgrid for Grid Connected and Islanded Operations," in *IEEE Transactions on Smart Grid*, vol. 6, no. 4, pp. 1588-1601, July 2015.

[5] X. Tang, X. Hu, N. Li, W. Deng and G. Zhang, "A Novel Frequency and Voltage Control Method for Islanded Microgrid Based on Multienergy Storages," in *IEEE Transactions on Smart Grid*, vol. 7, no. 1, pp. 410-419, Jan. 2016.

[6] S. Grillo, V. Musolino, L. Piegari, E. Tironi and C. Tornelli, "DC Islands in AC Smart Grids," in *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 89-98, Jan. 2014.

[7] M. Corti, G. Superti-Furga, E. Tironi, A. M. Pavan and G. Sulligoi, "Intentional islanding in medium voltage distribution grids," *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, Florence, 2016, pp. 1-6.

[8] S. Negri, E. Tironi and D. S. Danna, "Integrated Control Strategy for Islanded Operation in Smart Grids: Virtual Inertia and Ancillary Services," in *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2401-2411, May-June 2019.

[9] S. Negri, E. Tironi and G. Ubezio, "Zonal DC Distribution System based on Multiport Converters: Fault Analysis and Protection Design," *2019 IEEE Milan PowerTech*, Milan, 2019.

[10] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids - A General Approach Toward Standardization", in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 158-172, Jan. 2011.

[11] A. Tavakoli, M. Negnevitsky and K. M. Muttaqi, "A Decentralized Model Predictive Control for Operation of Multiple Distributed Generators in an Islanded Mode," in *IEEE Transactions on Industry Applications*, vol. 53, no. 2, pp. 1466-1475, March-April 2017.

[12] A. La Bella, S. Raimondi Cominesi, C. Sandroni and R. Scattolini, "Hierarchical Predictive Control of Microgrids in Islanded Operation," in *IEEE Transactions on Automation Science and Engineering*, vol. 14, no. 2, pp. 536-546, April 2017.

[13] A. La Bella, S. Negri, R. Scattolini and E. Tironi, "A Two-Layer Control Architecture for Islanded AC Microgrids with Storage Devices," *2018 IEEE Conference on Control Technology and Applications (CCTA)*, Copenhagen, 2018, pp. 1421-1426

[14] S. Khosrogorji, M. Ahmadian, H.Torkaman, "Multi-input DC/DC converters in connection with distributed generation units – A review", *Renewable and Sustainable Energy Reviews*, vol. 66, pp. 360-379, Dec 2016.

[15] Z. Rehman, I. Al-Bahaly, S. Mukhopadhyay, "Multiinput DC–DC converters in renewable energy applications – An overview", *Renewable and Sustainable Energy Reviews*, vol. 41, pp. 521-539, Jan 2015

[16] N.Zhang, D. Sutanto, K. M. Muttaqi, "A review of topologies of three-port DC–DC converters for the integration of renewable energy and energy storage system", *Renewable and Sustainable Energy Reviews*, vol. 56, pp. 388-401, April 2016

[17] P. Veena, V. Indragandhi, R. Jeyabharath, V.Subramaniyaswamy, "Review of grid integration schemes for renewable power generation system", *Renewable and Sustainable Energy Reviews*, vol. 34, pp. 628-641, June 2014

[18] W. Jiang and B. Fahimi, "Multiport Power Electronic Interface—Concept, Modeling, and Design," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1890-1900, July 2011.

[19] P. Shamsi and B. Fahimi, "Dynamic Behavior of Multiport Power Electronic Interface Under Source/Load Disturbances," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4500-4511, Oct. 2013.

[20] M. Corti, E. Tironi and G. Ubezio, "Multi-port converters in smart grids: Protection selectivity," *2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Anacapri, 2016, pp. 143-149.

[21] S. Danyali, S.A.K.H. Mozaffari Niapour, S.H. Hosseini, G.B: Gharehpetian, M. Sabahi. "New Single-Stage Single-Phase Three-Input DC-AC Boost Converterfor Stand-Alone Hybrid PV/FC/UC Systems", *Electric Power Systems Research,* vol. 127, pp. 1-12, Oct 2015.

[22] R. Faraji, E. Adib, H. Farzanehfard, "Soft-switched non-isolated high step-up multi-port DC-DC converter for hybrid energy system with minimum number of switches", *International Journal of Electrical Power and Energy Systems*, vol 106, pp. 511-519, March 2019

[23] S. Negri, E. Tironi and G. Ubezio, "Local DC Distribution System in Presence of RES and Storage Devices: Multiport Converters Application," *2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe)*, Palermo, 2018, pp. 1-8.

[24] C. Zhao, S. D. Round and J. W. Kolar, "An Isolated Three-Port Bidirectional DC-DC Converter With Decoupled Power Flow Management," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2443-2453, Sept. 2008.

[25] J. Schäfer, D. Bortis and J. W. Kolar, "Multi-port multi-cell DC/DC converter topology for electric vehicle's power distribution networks," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-9

[26] W. Li, J. Xiao, Y. Zhao and X. He, "PWM Plus Phase Angle Shift (PPAS) Control Scheme for Combined Multiport DC/DC Converters," in *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1479-1489, March 2012.

[27] K. Itoh, M. Ishigaki, N. Yanagizawa, S. Tomura and T. Umeno, "Analysis and Design of a Multiport Converter Using a Magnetic Coupling Inductor Technique," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1713-1721, March-April 2015.

[28] H. Wu, K. Sun, L. Zhu and Y. Xing, "An Interleaved Half-Bridge Three-Port Converter With Enhanced Power Transfer Capability Using Three-Leg Rectifier for Renewable Energy Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 606-616, June 2016.

[29] L. Kumar, S.Jain, "A multiple source DC/DC converter topology", *International Journal of Electrical Power and Energy Systems*, vol 51, pp. 278-291, Oct 2013

[30] H. Zhu, D. Zhang, H. S. Athab, B. Wu and Y. Gu, "PV Isolated Three-Port Converter and Energy-Balancing Control Method for PV-Battery Power Supply Applications," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 6, pp. 3595-3606, June 2015.

[31] V. N. S. R. Jakka, A. Shukla and G. D. Demetriades, "Dual-Transformer-Based Asymmetrical Triple-Port Active Bridge (DT-ATAB) Isolated DC–DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4549-4560, June 2017.

[32] Z. Qian, O. Abdel-Rahman and I. Batarseh, "An Integrated Four-Port DC/DC Converter for Renewable Energy Applications," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1877-1887, July 2010.

[33] H. Wu, J. Zhang and Y. Xing, "A Family of Multiport Buck–Boost Converters Based on DC-Link-Inductors (DLIs)," in *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 735-746, Feb. 2015.

[34] E. Tironi, M. Corti and G. Ubezio, "A novel approach in multi-port DC/DC converter control," *2015 International Conference on Clean Electrical Power (ICCEP)*, Taormina, 2015, pp. 48-54.

[35] M. Corti, E. Tironi and G. Ubezio, "DC Networks Including Multiport DC/DC Converters: Fault Analysis," in *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 3655-3662, Sept.-Oct. 2016.

[36] M. S. Carmeli, F. Castelli-Dezza and G. Superti-Furga, "Constant frequency current modulation algorithm based on linkage flux," *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, 2003, pp. 195-200 vol.1.

[37] M. S. Carmeli and G. Superti-Furga, "Direct current control of multilevel drive with novel floating capacitor control," *3rd Renewable Power Generation Conference (RPG 2014)*, Naples, 2014, pp. 1-6.

[38] V. I. Utkin, "Sliding mode control design principles and applications to electric drives," in *IEEE Transactions on Industrial Electronics*, vol. 40, no. 1, pp. 23-36, Feb. 1993.

[39] V. I. Utkin, "Sliding mode control of DC/DC converters", *Journal of the Franklin Institute*, vol 350, n. 8, pp. 2146-2165, Oct 2013

[40] Y. B. Shtessel, O. A. Raznopolov and L. A. Ozerov, "Control of multiple modular DC-to-DC power converters in conventional and dynamic sliding surfaces," in *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 45, no. 10, pp. 1091-1100, Oct. 1998.

[41] Michele Cucuzzella, Riccardo Lazzari, Sebastian Trip, Simone Rosti, Carlo Sandroni, Antonella Ferrara, "Sliding mode voltage control of boost converters in DC microgrids", *Control Engineering Practice*, vol 73, pp. 161-170, April 2018

[42] M. S. Carmeli, F. Castelli-Dezza and G. Superti-Furga, "Generalized Decoupling Method for Current-Controlled Multiswitching Systems," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 348-359, Feb. 2009.

[43] M. S. Carmeli, G. Superti-Furga. "Augmented State Approach in Quasi-Sliding-Mode Controlled PEBB Based Power Converters", *Int. Journal of Emerging Electric Power Systems,* vol. 15, no. 4, Aug 2014, pp. 335-347.

[44] V. I. Utkin, "Sliding Modes in Control and Optimization", *Springer-Verlag,* 1992.

[45] H. K. Khalil, "Nonlinear Systems", *Prentice Hall*, 1996.

[46] J. E. Slotine, W. Li "Applied Nonlinear Control", *Prentice Hall*, 1991.

[47] V. I. Utkin, J. Guldner, J. Shi, "Sliding Mode Control in Electro-Mechanical Systems", *CRC Press,* 2009.

[48] K. P. Jankowski, "Inverse Dynamic Control in Robotic Applications", Trafford, 2004.

[49] G. P. Incremona, M. Rubagotti and A. Ferrara, "Sliding Mode Control of Constrained Nonlinear Systems," in *IEEE Transactions on Automatic Control*, vol. 62, no. 6, pp. 2965-2972, June 2017.

[50] P. Albertos, A. Sala, "Multivariable Control Systems: An Engineering Approach", *Springer-Verlag*, 2004.