A MEMS Real-Time Clock with Single-Temperature Calibration and Deterministic Jitter Cancellation

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***Abstract*—This paper presents a Real-Time Clock (RTC) system, based on a microelectromechanical system (MEMS) resonator coupled to a integrated circuit (IC) that implements a frequency-compensating machine. The MEMS resonator is built with a standard, industrial-grade polysilicon process characterized by a $-30\,\mathrm{ppm/K}$ linear Temperature-Coefficient of Frequency (TCf) and the frequency-drift compensation is entirely carried out within the IC by means of a fractional frequency division. The large, but deterministic, output jitter ($\approx 1\,\mu s_{rms}$) is then suppressed down to less than $40\,ns_{rms}$ with a low-power Digital-to-Time Converter (DTC), whose usefulness in this kind of application is then analyzed. With a single-point temperature calibration, a $\pm 8\,\mathrm{ppm}$ output frequency stability is demonstrated at $\approx 800\,\mathrm{nA}$ current consumption from a $1.2\,\mathrm{V}$ supply.**

***Index Terms*—RTC, MEMS, DTC, jitter, low-power electronics.**

I. Introduction

REAL-TIME CLOCKS have been a fundamental block for embedded electronics for decades. Typical features of temperature-compensated RTCs based on quartz resonators are providing a 32.768 kHz time-base for computing systems at $\pm 10\,\mathrm{ppm}$ frequency stability, acceptable current consumption in the order of 1 µA and tens of ns rms jitter [1], [2]. Significant improvements have been achieved in terms of understanding the properties of quartz and optimizing the geometry, size and performance of tuning fork resonators. Nevertheless, in recent years microelectromechanical systems (MEMS) have matured enough to propose an alternative to quartz resonators [3]–[6]. On one hand, MEMS devices typically suffer from larger frequency drift due to temperature variations and poorer power handling. On the other hand, MEMS resonators can be fabricated with CMOS compatible processes, can be packaged in a smaller size and can be assembled together with an integrated circuit that performs a compensation of the output frequency.

Past works mostly investigated the use of MEMS devices based on a specifically-tailored process that reduced the native drift of the MEMS resonator and relaxed the constraints posed on the compensating electronics, in any case necessary to match the stability performances of quartz-based RTCs. However, the part-to-part spread on the thermal dependence of the frequency is large to the point where each clock must be calibrated on several temperature points. This makes lengthy and expensive calibration routines necessary, thus slowing fabrication times and increasing the part cost.

In the present work, another approach is investigated, which starts from the consideration that epitaxial-polysilicon resonators built in a mature and industrial-grade MEMS process show a more repeatable behavior in their (larger) thermal frequency drift [7]. The reduction in the calibration costs and time may be appealing in an application where a significantly faster calibration routine, hence cheaper parts and larger volumes, can be traded with an overall slightly degraded thermal stability. Therefore, a dedicated IC is developed, which includes an oscillator, a fractional frequency divider to compensate the drift of such MEMS resonators and an additional block to suppress the jitter at the system output based on a novel low-power deterministic jitter cancellation.

To describe the implemented system, the paper is organized as follows: Section II discusses the possible compensation strategies and the effects of the calibration routine, Section III presents the reference oscillator and the employed MEMS resonator, Section IV describes in detail the used frequency-compensating blocks and analyzes an alternative approach to the filtering of the jitter introduced by the ΣΔ modulation, Section V reports the design of the jitter suppressing block, Section VI shows the measurement results and, finally, Section VII compares the proposed jitter suppressing strategy with the use of a commonly adopted phase-locked loop (PLL) filtering.

II. Single-Point Calibration and Compensation

Several studies have investigated the temperature stability of Single-Crystal Silicon (SCS) resonators. Two main strategies to stabilize the MEMS resonators have been highlighted. The first one combines materials with opposite TCf to achieve a flat temperature dependence, to first order [8]. The second, and more widespread, solution focuses on achieving optimal dopant density and orientation of the device with respect to the crystallographic axes to achieve the same goal [9].

Nonetheless, an overall output frequency drift of $\pm 10\,\mathrm{ppm}$ can be achieved only if a further compensation is carried out with a dedicated electronic circuit, such as in [10], [11]. This electronic system, depicted in Fig. 1, relies on a reference oscillator running at a larger frequency than the standard output frequency of 32.768 kHz. This frequency is then the input of a multi-modulus divider, that can change its division modulus between N and $N + 1$ according to its Modulus Control (MC) input. By changing the proportion of divisions

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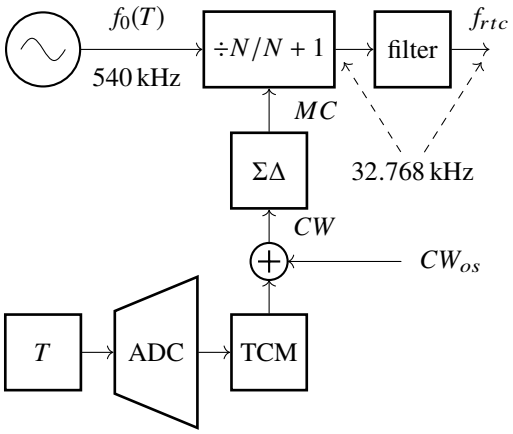


Fig. 1. RTC system-level architecture: the 540 kHz reference frequency from the MEMS-based oscillator is divided by the multi-modulus divider, by N or $N+1$ according to the Modulus Control (MC) input, down to the correct average frequency of 32.768 kHz. The Command Word CW is produced by a temperature sensing chain and is ΣΔ-modulated at the MC output. A phase filter can be introduced before the final output to clean the jitter introduced by the ΣΔ modulation.

by the two available moduli, a fine range of *average* output frequencies can be achieved. The MC signal is obtained as a result of a single-bit ΣΔ modulation of the Command Word (CW) signal, a digital multi-bit signal that encodes the fractional part of the desired division factor to compensate for the temperature variation, sensed with an on-chip sensor, and the initial frequency spread due to fabrication tolerances.

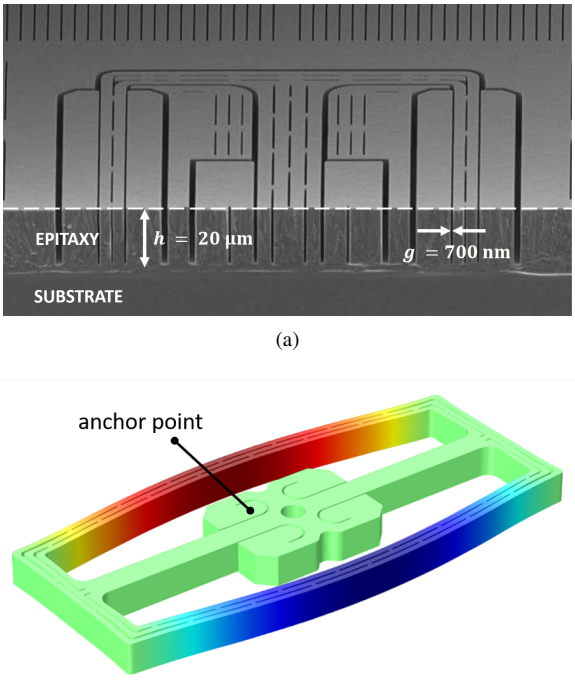
A heavily-doped SCS mechanical structure with a further electronic compensation has been used, for example, in [10], where a ≈50 ppm part-to-part spread in the frequency versus temperature characteristics of the MEMS resonators requires a five-point calibration in temperature to achieve the target frequency stability, a long and inconvenient procedure. Conversely, it is shown in [12] that a better part-to-part spread can be achieved if standard, lowly-doped polysilicon resonators, characterized by a worse −30 ppm/K TCf, are employed instead. The same work suggests the use of a just 1-point calibration (i.e. a compensation of the frequency offset at room temperature) to achieve adequate frequency accuracies. This quicker, simplified calibration would lead directly to a great benefit in the reduction of calibration costs and is the approach followed in the present work.

Referring again to Fig. 1, since typical process-induced frequency spread $\left.\frac{\Delta f}{f}\right|_p$ at room temperature are significantly larger than the maximum thermal drift, the choice of N is merely derived as:

$$\left.\frac{\Delta f}{f}\right|_p < \frac{f_{max}-f_{min}}{\frac{f_{max}+f_{min}}{2}} = \frac{\frac{f_0}{N}-\frac{f_0}{N+1}}{\frac{f_0}{N+\frac{1}{2}}} \Rightarrow N < \frac{1}{\left.\frac{\Delta f}{f}\right|_p} - \frac{1}{2} \quad (1)$$

where f_{max} (f_{min}) is the maximum (minimum) of the frequency distribution around the mean value f_0. In this work $N = 16$ was used, so that a maximum ±3 % frequency offset can be compensated.

The granularity of the frequency compensation $\frac{\Delta f}{f}$ is set by the number of bits B of the ΣΔ modulator. Given a maximum



(a)

(b)

Fig. 2. The MEMS capacitive resonator used in the present work, after a vertical cut before the oxide release, is shown in (a). The visible slots in the resonant elements enhance the quality factor of the resonator by reducing energy losses due to thermo-elastic damping. In (b) the resonant mode of interest of the MEMS device, nominally at 540 kHz, is represented.

deviation of the division modulus of $1/N$, B is required to be:

$$\frac{\Delta f}{f} = \frac{1}{N \cdot 2^B} \Rightarrow B = -\log_2\left(N \cdot \frac{\Delta f}{f}\right) \quad (2)$$

The ΣΔ modulator needs 13 bits to achieve an ideal output frequency granularity of 7 ppm.

Finally, the TCM of Fig. 1 implements the compensation law identified in [12]:

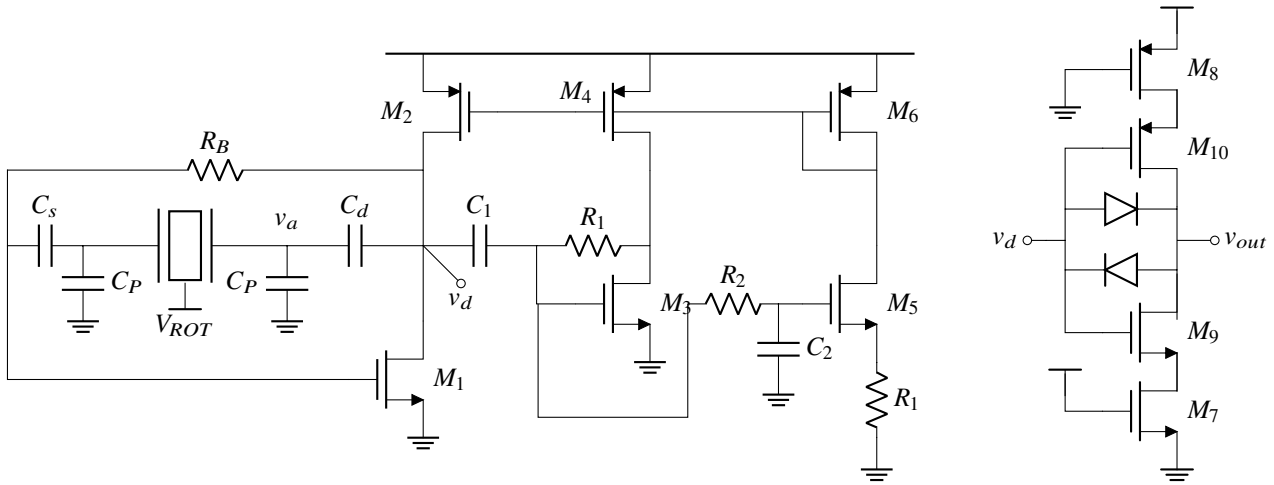
$$f(T) = f_0\left[1 - 30.86\times10^{-6}(T-T_0) - 0.024\times10^{-6}(T-T_0)^2\right] \quad (3)$$

which is characteristic of the used epitaxial polysilicon process where $T_0 = 27\,^{\circ}\mathrm{C}$.

III. Reference Oscillator

A. MEMS Resonator

The devices used for this work are capacitive polysilicon resonators realized in the ThELMA process by STMicroelectronics, an industrial micromachining mainly used for capacitive inertial sensors [13]. The target resonant frequency is 540 kHz, i.e. (N+0.5)×32.768 kHz. The mechanical design, shown in Fig. 2, is similar to that described in [12], but with tighter gaps, as narrow as 700 nm, so that the nominal motional resistance R_m is reduced to ≈100 kΩ, with a rotor voltage of 2.4 V, at a vacuum level in the order of 50 µbar, low enough to make thermo-elastic damping the dominant source of dissipation. Another consequence of the tighter gaps is an increased impact of the non-linear mechanism associated to the electrostatic stiffness. In fact, in [12] the amplitude of the



(a) In the core of the oscillator, the two C_P capacitors between the MEMS drive/sense ports and ground represent the combination of the parasitic capacitance of the I/O pads and the active and parasitic capacitances present within the MEMS device.

(b) The output buffer squares the oscillating signal taken at the drain of the transconductor of the Pierce oscillator v_d.

Fig. 3. Schematic of the oscillator subdivided in sustaining amplifier and output buffer.

driving voltage that constituted the boundary between linear and non-linear operation was found to be ≈80 mV. The new resonator with tighter gaps has a lower limit of roughly 10 mV so that variability in the amplitude of the MEMS displacement due to spreads in the actuation voltage, the gap and electrical components do not affect significantly the $f(T)$ law previously measured. This will impact the oscillator design, described in the following section. The design, with four anchor points in the device central region, minimizes effects of carrier/package-induced thermal stresses on the device in-plane gaps, thus minimizing the impact on the frequency caused by electrostatic softening. For more details about this design approach the reader can refer to [14], [15]. The first mode of the resonator is shown in Fig. 2b.

B. Oscillator Design

The described resonator was coupled to an integrated circuit (IC) implementing an oscillator and other temperature-compensating blocks that will be described in the following sections. The IC was implemented in a 130 nm 1P4M process with a supply voltage of 1.2 V.

A Pierce topology was chosen for the oscillator, since it does not need any low-impedance node for proper operation. This is a difficult condition to achieve at the required hundreds of nano-ampere level. An Automatic-Gain Control (AGC) circuit was adopted to keep the MEMS resonator within its linear operating range by controlling the amplitude of the driving voltage and to reduce as much as possible the steady-state power consumption. With respect to the standard Pierce circuit, a few modifications similar to [10], [12], [16] were made in the circuit schematic, shown in Fig. 3.

Firstly, two decoupling capacitors C_s and C_d were added in series with the MEMS terminals to maximize the transduction factor by applying the full voltage difference $V_{ROT} = 2.4$ V between the MEMS rotor and stator. This, in turn, minimizes the R_m and therefore minimizes the current required to operate the oscillator.

Secondly, the amplitude of the voltage that drives the MEMS resonator is lowered by the capacitive divider formed by $C_d = 45$ fF and the parasitic capacitance $C_P \approx 0.7$ pF. In this way, a large amplitude of about 100 mV (v_d) can be controlled by the AGC circuit more easily, whereas the MEMS resonator stays within its linear region ($v_a < 10$ mV). Moreover, this sinusoidal voltage with larger amplitude can be turned into a squarewave more easily.

Thirdly, the output comparator (Fig. 3b) was implemented as an inverter with a feedback network made with two anti-parallel diodes to bias the inverter (formed by M9 and M10) close to threshold while not adding too much loss conductance to the oscillator node. For the same reason, two resistors implemented by MOS transistors M7-M8 were added in series with the two sources of the inverter MOS transistors.

The AGC is sized by resorting to the characteristic equations that relate the oscillator bias current I_0 to voltage amplitudes in the Pierce oscillator. Derivation of such equations is based on [17]. The working point of the amplitude-controlled oscillator is then expressed by the following equation, relating the amplitudes of gate and drain voltages (v_g and v_d, respectively) to key bias current values:

$$\frac{I_0^{startup}}{I_{0,crit}}\left(1-\frac{\ln(\mathcal{I}_0(v_d))}{\ln(K_W)}\right)=v_g\frac{\mathcal{I}_0(v_g)}{2\mathcal{I}_1(v_g)} \tag{4}$$

where $I_0^{startup}$ is M1 bias current at start-up, set by the AGC and inversely proportional to resistor R_1, $I_{0,crit}$ is the critical current for oscillation, proportional to R_m, K_W is the mirror ratio between transistors M3 and M5, and $\mathcal{I}_0$ and $\mathcal{I}_1$ are the Bessel functions of order 0 and 1 respectively. The equation is evaluated graphically, as shown in Fig. 4, where the two characteristic equations are plotted as function of normalized gate amplitude and bias current. The working point is the intersection of these curves, and it corresponds to a

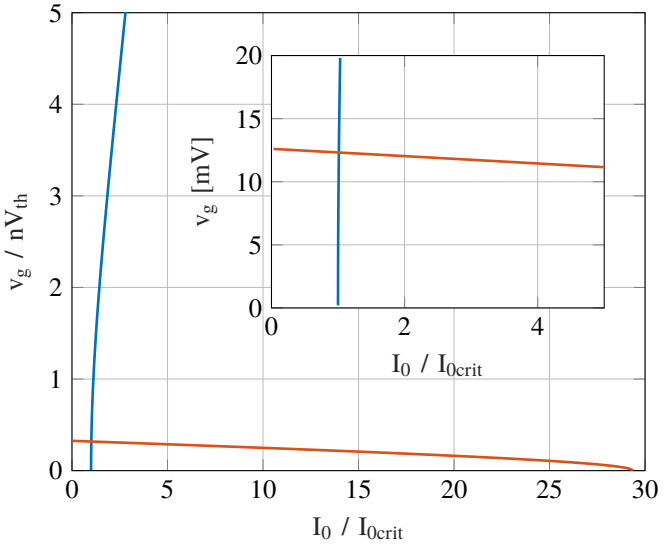


Fig. 4. Regulator operating point.

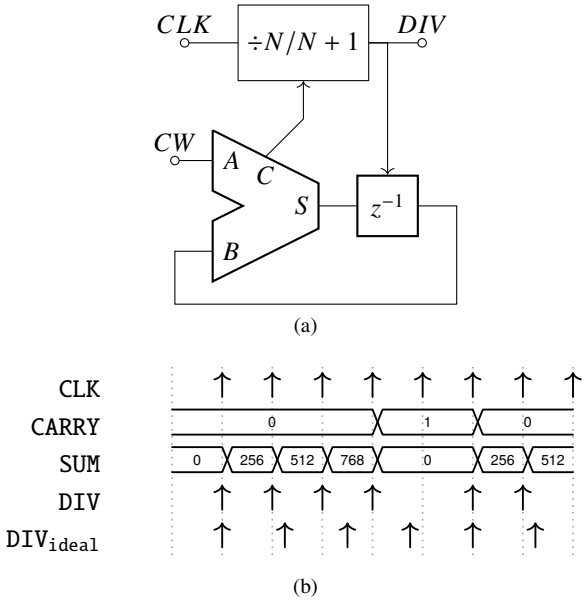


Fig. 5. Timing diagram (b) of the main signals involved in the ΣΔ modulation of the division modulus, whose block scheme is represented in (a). For the sake of simplicity, this is represented assuming a 10 bit accumulator, $CW = 256$ and $N = 1$, so that the division modulus can be 1 or 2. At each cycle, the SUM value is increased by CW, showing a sawtooth behavior. When an overflow happens, the carry becomes high and the following period of the DIV signal is extended by one clock period. DIV_{ideal} represents the time stamps of an ideal 32.768 kHz clock.

gate amplitude of roughly 12 mV with the adopted sizing. Accounting for process spread, resistor R_1 is made variable, in order to allow calibration of the start-up current prior to operation.

IV. System-Level Compensation

The frequency-compensation technique described in Section II adjusts on average the output frequency at the cost of an increased output jitter given by change in the instantaneous division factor between N and $N+1$. Nevertheless, its highly-digital nature makes it suited to a compensation algorithm of this additional jitter, which is not a stochastic process. This Section describes the theoretical background behind this aspect of the compensation system, whereas the implementation will be discussed in Section V.

A. Sigma-Delta operation

It has been shown that a digital accumulator can be used as a digital ΣΔ modulator [18]. In fact, as the input value gets accumulated, the larger the input value the more often an overflow happens. Therefore, it is intuitive to believe that the carry out bit is the ΣΔ modulation of the input CW. An example of this concept is illustrated with the relevant digital waveforms in Fig. 5, whereas a formal demonstration can be found in [18, pp. 67-68].

If one names $T_d(k)$ the sequence of the divided clock (DIV) periods, it is possible to demonstrate that:

$$T_d(k) = \frac{N(k)}{f_0} = \frac{N + \frac{CW}{2^B}}{f_0} - \frac{S(k) - S(k-1)}{2^B f_0} \qquad (5)$$

where $S(k)$ is the increasing value stored in the accumulator register, $k = 0, 1, 2, \ldots$ and B is the number of bits used in the modulator. The sequence $t_d(k)$ of the DIV edges is the integral of the period sequence, and is therefore:

$$t_d(k) = \sum_{i=0}^{k} T_d(i) = \frac{1}{f_0}\left[k\left(N + \frac{CW}{2^B}\right) - \frac{S(k)}{2^B}\right] \qquad (6)$$

One can note that in (6) there are two main terms: the first one, related to CW, expresses the control of the division modulus; the second one, related to $S(k)$, constitutes an undesired disturbance that ruins the purity of the output phase. Nonetheless, this jitter is known *a priori*, since it is proportional to the value $S(k)$ stored in the accumulator register. It is therefore possible to build a Digital-to-Time Converter (DTC) to introduce a proper delay to each edge of the divided signal to compensate for this error and keep the period jitter requirement within the specification. As can be inferred from (6), the DTC must be able to apply a maximum delay (Full-Scale Range, FSR) matched to $\frac{1}{f_0}$ and should be driven by $S(k)$.

This approach has been used in the past in several works [19]–[22], characterized by completely different requirements in terms of noise, power consumption and frequency of operation. Nonetheless, to the authors' knowledge this architecture has never been used in such an extremely power-constrained application like the ones presented in this work.

B. Jitter Evaluation

It is evident from (6) that, during the limit cycle of the ΣΔ modulator, the divided period $T_d(k) = t_d(k) - t_d(k-1)$ sequence can assume only two possible values, according to the presence or absence of an overflow within the accumulator. Specifically, it is possible to say that in a first-order modulator[1], over a limit cycle of 2^B periods (the cycle can also be shorter), when a

[1]Increasing the order of the modulator increases both the high-pass noise-shaping ability and the power consumption (even though the latter effect would be minor in this specific case). Since no phase-domain low-pass filter is used in this work, a better noise-shaping is not useful and therefore higher-order modulators are not discussed.

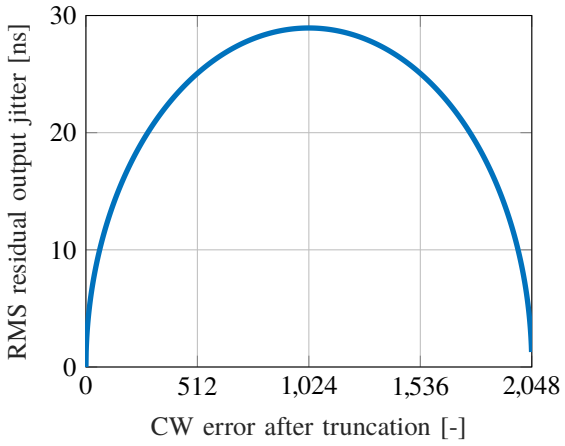


Fig. 6. Output RMS period jitter as a function of the truncated portion of the command word CW.

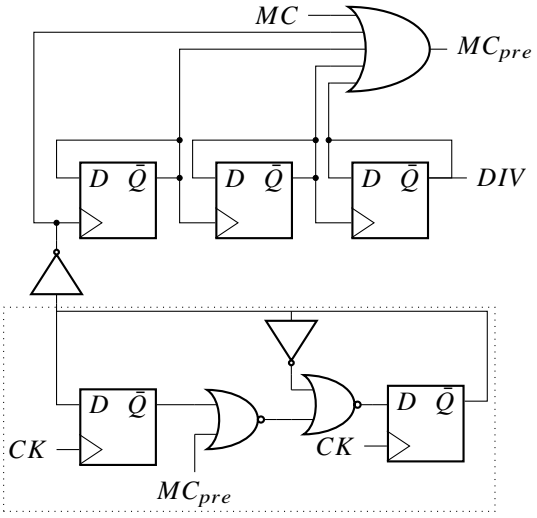


Fig. 7. Schematic of the multi-modulus divider: a ÷2/3 prescaler (in the dotted box) is then followed by three divide-by-2 flip-flops. The MC input, through the combinational logic, drives the evolution of the system in order to have a ÷16, or ÷17 behavior.

constant CW is used like in this case, the sequence of period jitter at the output of the divider $T_{d,\epsilon}(k) = T_d(k) - \frac{1}{f_{rtc}}$ will be:

$$T_{d,\epsilon} = \frac{1}{2^B f_0}[S(k) - S(k-1)] = \\ = \begin{cases} \frac{1}{2^B f_0} \cdot CW & \text{for } 2^B - CW \text{ times} \\ \frac{1}{2^B f_0}\left(2^B - CW\right) & \text{for } CW \text{ times} \end{cases} \tag{7}$$

Once the compensating delay is introduced, considering that only the first B_c bits of the error will be compensated (as explained at the end of this section), one obtains that the output jitter can assume, again, only two possible values. Introducing $\widetilde{CW}(k) = CW_{b-1:0}(k)$[2], $\widetilde{S}(k) = S_{b-1:0}(k)$ and $b = B - B_c$, one obtains:

$$T_{d,\epsilon} = \frac{1}{2^B f_0}[\widetilde{S}(k) - \widetilde{S}(k-1)] = \\ = \begin{cases} \frac{1}{2^B f_0} \cdot \widetilde{CW} & \text{for } 2^b - \widetilde{CW} \text{ times} \\ \frac{1}{2^B f_0}\left(2^b - \widetilde{CW}\right) & \text{for } \widetilde{CW} \text{ times} \end{cases} \tag{8}$$

Therefore, one can compute the rms period jitter σ_j as:

$$\sigma_j^2 = \overline{T_{d,\epsilon}^2} = \\ = \left(\frac{1}{2^B f_0}\right)^2 \frac{\widetilde{CW}^2 \cdot (2^b - \widetilde{CW}) + (2^b - \widetilde{CW})^2 \cdot \widetilde{CW}}{2^b} = \\ = \left(\frac{1}{2^B f_0}\right)^2 \left(2^b \cdot \widetilde{CW} - \widetilde{CW}^2\right) \tag{9}$$

Then, the worst-case period jitter σ_j^{wc} is obtained when $\widetilde{CW} = 2^{b-1}$ and is equal to:

$$\sigma_j^{wc} = \frac{1}{2^{B-b} f_0} = \frac{1}{2^{B_c} f_0} \tag{10}$$

[2]The syntax $A_{m-1:0}$ indicates the value assumed by the digital word formed by the m least significant bits of signal A.

Finally, the required number of bits B_c for the compensating DTC can be found as the one that is able to keep σ_j^{wc} below the requirement:

$$B_c > \log_2\left(\frac{1}{f_0 \cdot \sigma_j^{wc}}\right) \tag{11}$$

Considering the present case where $\frac{1}{f_0} = 1.85\,\mu s$ and $\sigma_j < 35\,ns$ from initial specifications, one can find $B_c = 5$. One can also compensate with more bits than the minimum available, thereby decreasing the output jitter, but (i) this trades with increased power consumption and silicon area and (ii) is limited by the magnitude of the divided oscillator jitter.

The output jitter as a function of the truncation error, expressed by (9), is represented in Fig. 6 in the case of $B_c = 5$.

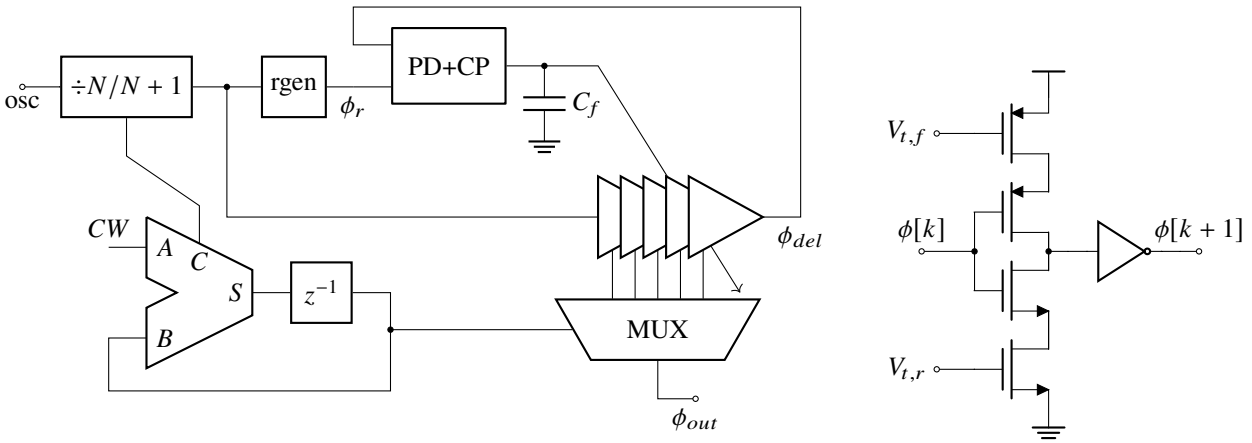
V. Design of Compensating Electronics

A. Divider Design

The multi-modulus divider is based on an efficient asynchronous architecture similar to [23], to use minimal hardware clocked at the maximum frequency. As it is the digital block with the highest switching activity, it was designed prioritizing the reduction of its power consumption. To do so, the whole digital section was powered at 0.8 V and custom logic gates were partly used to further reduce the consumption. With reference to the schematic of the divider shown in Fig. 7, the prescaler employs dynamic flip flops, whereas the subsequent dividing flip-flops, clocked at increasingly slower frequencies, are static to prevent leakages at high temperatures from erasing the sampled datum.

B. DTC Design

As discussed in Section IV, the FSR of the DTC should match $1/f_0$. According to behavioral simulations of the compensation system, an error in the FSR larger than 1 LSB =



(a) Block scheme of the compensating architecture. (b) Schematic of the delay cell.

Fig. 8. Block scheme of the whole frequency/phase compensating circuit. The loop around the variable-delay chain is doubled so as to compensate the output jitter on both the rising and falling output edges.

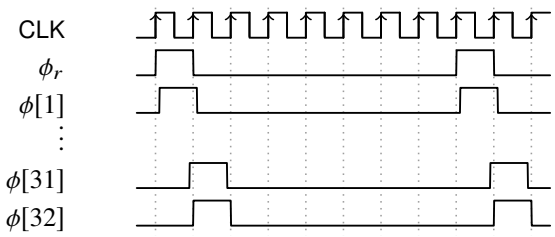


Fig. 9. Timing diagram of the digital signals employed in the DTC. For illustration purposes a periodicity of 8 rather than the actual 16 is used.

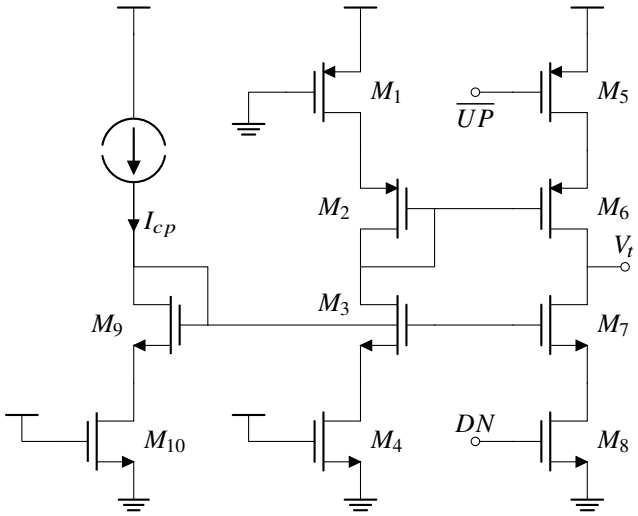


Fig. 10. Schematic of the charge pump circuit used [27]

$\frac{1}{f_0 \cdot 2^{B_c}}$ has detrimental consequences on the residual output jitter. To obtain this level of accuracy without any calibration, the FSR must be matched with a feedback system. In this work, a chain of $2^{B_c} = 32$ delay elements was used to create 32 replicas of the divided signal increasingly delayed. This chain was enclosed within a Delay-Locked Loop (DLL) that matches, with closed-loop operation, the full scale delay, i.e. the FSR, with the reference period $1/f_0$ [24]. The whole system is shown in Fig. 8.

It was noticed from simulations that a DLL clocked at f_{ref} would burn too much power, more than the 1 µA consumption required for the whole system. Therefore a slower DLL reference signal ϕ_r was derived, as shown in Fig. 9. A combinational network produces the ϕ_r squarewave signal at frequency f_{rtc} but with a 'high' duration equal to $\frac{1}{f_0}$. In this way, the PD can measure the time difference between the falling edge of ϕ_r and the rising edge of ϕ_{del} and the total delay of the chain is matched to $\frac{1}{f_0}$. The switching activity of the digital circuit is reduced by a factor of $N = 16$.

This results in a reference signal with a duty cycle very different from 50 %, which makes not viable the use of phase detectors based on XOR gates or latches, popular choices for DLL circuits [25], [26]. Therefore, the Phase-Frequency Detector (PFD) based on two flip-flops, typical of analog Phase-Locked Loops, was used, since it does not pose any requirement on the input duty cycle. Nevertheless, this brings up the problem of the false lock-up, for which the DLL may lock the edges of ϕ_{del} to the wrong edge of ϕ_r. This problem was solved by introducing a reset of the PFD after the non-sensitive edge of the divided signal ϕ_d.

To compensate the jitter on both the rising and falling edges of the output signal, the loop depicted in Fig. 8a is duplicated with a variable-delay element that implements two tuning inputs that act separately on the two edge polarities. The unit delay cell was implemented as shown in Fig. 8b. The delay is controlled by means of the two tuning voltages $V_{t,r}$ and $V_{t,f}$ – they act on the rising and falling edges respectively – that starve the commutation of the inverter formed by the two central transistors. The sizing of the transistors is a compromise between power consumption and matching of the delay units. The 32 phases thus created are then brought to the output through a multiplexer formed by a tree of tri-state inverters activated according to the $S(k)$ code.

The charge pump is implemented as a structure similar to [27], reported in Fig. 10 for the reader's convenience, and has a static consumption on the rightmost branch of I_{cp}. Any offset charge Q_{os} injected in the loop filter, formed by a single capacitor, has a direct impact on the achieved FSR of the

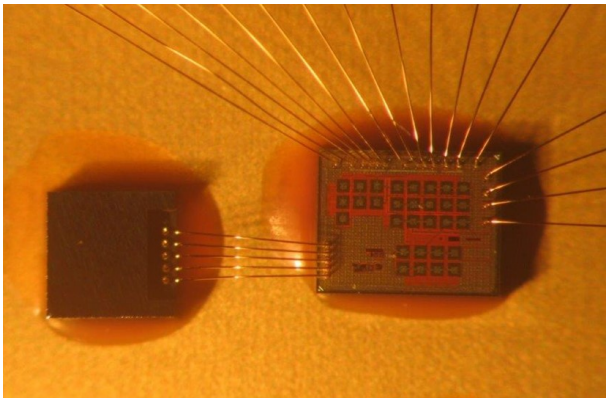


Fig. 11. Photo of the IC coupled to the MEMS. They were assembled on a ceramic package.

DTC. In fact, Q_{os} is directly translated as an error on the FSR through the $I_{cp}/2\pi$ gain of the PFD:

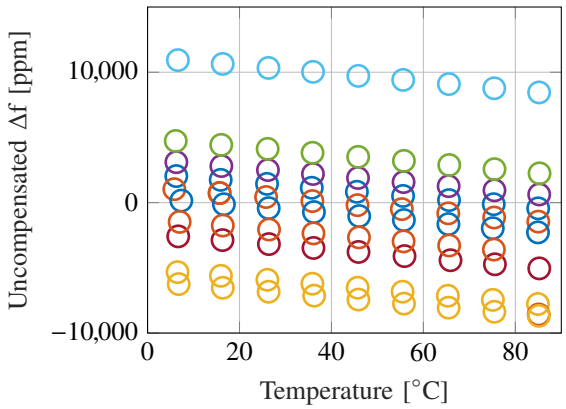
$$FSR_\epsilon = \frac{Q_{os}}{T_{rtc}} \cdot \frac{2\pi}{I_{cp}} \cdot \frac{T_{rtc}}{2\pi} \tag{12}$$

where $T_{rtc} = 1/f_{rtc} = 30.5\,\mu s$. From simulation, to keep FSR_ϵ within the 1 LSB requirement, I_{cp} was set to 40 nA.

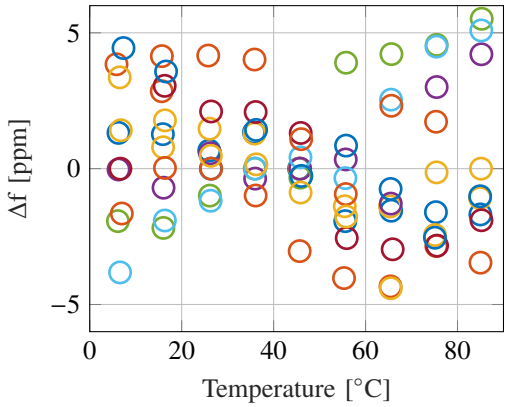
VI. Measurements

The described RTC system was fabricated and tested, coupled through wire-bonding to the aforementioned MEMS resonator, as shown in Fig. 11. Since the temperature sensor was not implemented in this IC, the compensation is provided with a microcontroller that acquires the temperature from the on-board sensor and computes real-time the correct CW. The temperature sensor was placed ≈5 mm far from the resonator and has a worst-case inaccuracy of <0.4 °C. The TCM was programmed with the same coefficients used in [12] and, for each MEMS, a single-point temperature calibration was used. The frequency stability of the system was tested within a climatic chamber over the 5 °C to 85 °C temperature range exploiting an on-board commercial temperature sensor. Before taking a measurement, the chamber was left idle for ≈20 min waiting for the overall temperature to settle. The on-chip compensation circuitry was initially bypassed. The result is shown in Fig. 12a: the trend is, as expected, dominated by a linear ≈ -30 ppm/K TCf and the frequency offset measured across 10 samples is about ±8500 ppm at each temperature point. The average $f(T)$ law measured in [12] was then applied, together with a single-point calibration at room temperature: the result is shown in Fig. 12b. An overall part-to-part spread of ±6 ppm can be observed over the same 10 samples.

The chip consumes a total of 642 nA, subdivided between 430 nA from the reference oscillator and 212 nA from the compensating circuitry, i.e. the multi-modulus divider, the ΣΔ modulator and the DTC. The chart in Fig. 13 represents the total consumption of the system broken down to its main contributors, together with a compatible temperature sensor with 25 mK resolution and 38 nJ energy-per-conversion taken from literature [10].



(a) Native frequency versus temperature characteristic of the reference oscillator. The measurement is repeated for the 10 samples (MEMS and IC) shown.



(b) The same $f(T)$ traces of Fig. 12a are compensated through a single-point calibration and a post-elaboration with the average law measured in [12]. With respect to [12], an improvement from ±20 ppm to ±6 ppm can be noted, which is to ascribe to the use of a more stable climatic chamber.

Fig. 12. Temperature stability with and without compensation.

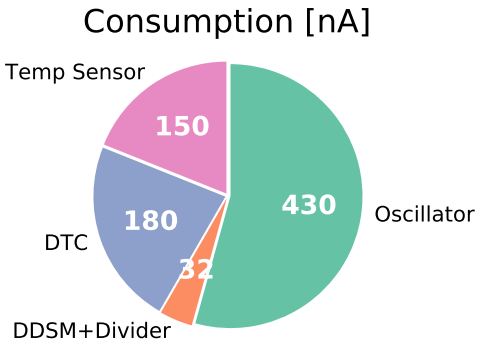


Fig. 13. Consumption of the chip split in the different blocks. The chart takes into account the consumption of the temperature sensor by multiplying the 38 nJ energy-per-conversion of a compatible temperature sensor [10] multiplied by the required sampling rate of 4 Hz.

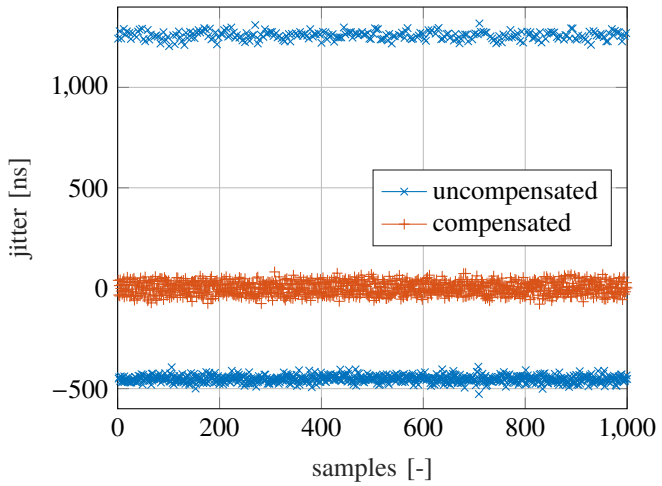


Fig. 14. Time traces of the output uncompensated and compensated jitter. The uncompensated trace shows a bi-modal distribution and its peak-to-peak deviation is equal to $1/f_0$ and is independent of the used CW. A proper compensation removes most of the deterministic portion of the jitter, so that the compensated trace becomes unimodal.

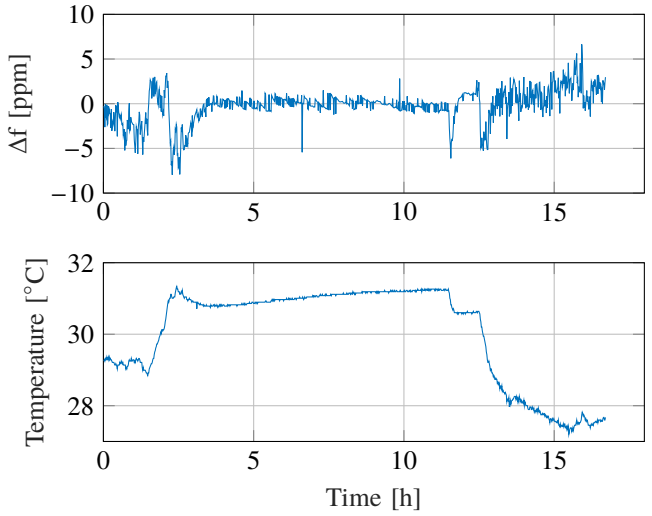


Fig. 15. Output frequency compensated in real-time with an external temperature acquisition chain. The ambient temperature is not controlled, the largest fluctuation are due to the automatic switching on/off of the air conditioning of the room.

The jitter suppression strategy was validated by measuring, for all the swept temperatures, the output jitter over 10 000 cycles with and without the DTC block. With $CW = AAAA$ (hexadecimal), a close to worst-case scenario as far as jitter is concerned, the jitter is suppressed from 944 ns_{rms} down to 31 ns_{rms} on average. The relative time traces are shown in Fig. 14.

A final experiment shows in Fig. 15 the compensated output frequency of the RTC system and its temperature when left in an uncontrolled environment for a long period of time. The frequency stays within ±8 ppm, with an observable sensitivity to temperature gradients due to different thermal transients between the packaged sensor and the IC. Such an effect is expected to largely disappear with an on-chip temperature sensor.

VII. PLL/DLL Comparison

From the electronic point of view, the major novelty of the proposed work lies in the adoption of a deterministic jitter compensation at ultra-low-power instead of a low-pass filtering with a PLL. This section will carry out a conceptual comparison between the two different filtering strategies. Specifically, this will be done by comparing the noise/jitter versus power trade-off.

A filtering PLL and the proposed DTC, based on a DLL, share a quite similar topology. Both have an input phase detector that produces the error signal and a loop filter that produces the tuning signal that controls the voltage-controlled oscillator (in a PLL) or a variable-delay element (in a DLL).

Therefore, a strategy that optimizes the noise and power consumption of the phase detector or the loop filter will be beneficial in roughly the same way in both solutions. It is therefore possible to compare the two strategies referring only to the two blocks that set apart the two architectures: the Voltage-Controlled Oscillator (VCO) and the delay chain.

The bandwidth of a PLL is constrained to be much smaller than its reference frequency, to filter as much as possible the very large noise introduced by the fractional divider. As a result, the high-pass filtered VCO noise will appear at the output of the system practically unfiltered.

To compute the period jitter σ_j of a generic ring VCO – the most popular choice at such low frequencies – one can resort to the approximation derived in [30]:

$$\sigma_j^2 = \frac{kT}{I f_0}\left[\frac{2}{V_{DD}-V_{TH}}\left(\gamma_n+\gamma_p\right)+\frac{2}{V_{DD}}\right] \tag{13}$$

where k is the Boltzmann constant, T the absolute temperature, V_{DD} the supply voltage, V_{TH} is the threshold voltage of the MOS transistors and γ_n and γ_p the noise factors for NMOS and PMOS respectively.

If a certain jitter σ_j is required, one finds that the current I_v that the VCO requires to reach the σ_j jitter amounts to:

$$I_v = \frac{kT}{\sigma_j^2 f_{rtc}}\left[\frac{2}{V_{DD}-V_{TH}}\left(\gamma_n+\gamma_p\right)+\frac{2}{V_{DD}}\right] \tag{14}$$

The noise introduced by the delay chain can be described by the same formula, since in the derivation of (13) the fact that the inverter chain is closed in loop does not affect the period jitter estimation. As a result, the current I_d required by the delay chain is:

$$I_d = \frac{kT}{\sigma_j^2 \frac{f_0}{2}}\left[\frac{2}{V_{DD}-V_{TH}}\left(\gamma_n+\gamma_p\right)+\frac{2}{V_{DD}}\right]\frac{f_{rtc}}{f_0} \tag{15}$$

Finally, the deterministic jitter compensation allows one to consume less power in the delay chain than in the VCO of a PLL used as a low-pass filter at equal output jitter by a factor:

$$\frac{I_v}{I_d} = \left(\frac{f_0}{f_{rtc}}\right)^2 = 135 \tag{16}$$

This is an ideal limit: the practical advantage is reduced by the need of proper matching of the unit delays, which calls for larger transistors and higher power consumption and leads to the overall DTC consumption of 180 nA.

	This work	[6]	[11]	[28]	[29]
Resonator	**Poly MEMS**	SCS doped MEMS	Piezo MEMS	Quartz	Quartz
Consumption [nA]	**642 (ext. T sensor)**	1000	3200	240	300
$\Delta f/f$ [ppm]	**±10**	±3	±10	±3	148
Period jitter [ns_{rms}]	**31**	35	n/a	n/a	n/a
Trimming points	**1**	5	3	n/a	n/a

TABLE I
COMPARISON OF THE RTC PRESENTED IN THIS PAPER WITH OTHER COMPARABLE REFERENCES.

VIII. CONCLUSION

This work presents a RTC system composed by a polysilicon MEMS resonator coupled to a novel integrated circuit that implements a low-power oscillator and the blocks necessary for the frequency and phase compensation of the oscillatory signal. A RTC with 642 nA overall consumption, ±8 ppm maximum frequency drift and 35 ns_{rms} output jitter was proved.

Table I provides a comparison with other academic and commercial references. The higher $-30\,\text{ppm/K}$ TCf_1 of the proposed RTC can make the RTC operation more critical under strong thermal gradients, but, unfortunately, due to the external temperature sensor a fair comparison cannot be shown at the moment. Nonetheless, typical quartz or MEMS natively-compensated resonators show a TCf_1 of 4-6 ppm/K at the boundaries of the thermal operating range, so that the difference in performance can be less dramatic than what one could expect, and could be compensated by a higher temperature sampling rate.

Additionally, a novel approach to short-term jitter suppression was proposed, analyzed, implemented and verified. The technique is based on a cancellation of the known jitter introduced by the ΣΔ modulation by means of a Digital-to-Time Converter, and is proved to be more efficient than a low-pass filter implemented as a PLL with a ring VCO.

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