Electrical Conductance of Silicon Photonic Waveguides

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Compiled November 4, 2020

Many optoelectronic devices embedded in a silicon photonic chip, like photodetectors, modulators and attenuators, rely on waveguide doping for their operation. However, the doping level of a waveguide is not always reflecting in an equal amount of free carriers available for conduction, because of the charges and trap energy states inevitably present at the Si/SiO_2 interface. In a Silicon-On-Insulator technology with 10^{15} cm^{-3} p-doped native waveguides this can lead to a complete depletion of the core from free carriers and to a consequent very high electrical resistance. This letter experimentally quantifies this effect and shows how the amount of free carriers in a waveguide can be modified and restored to the original doping value with a proper control of the chip substrate potential. A similar capability is also demonstrated by means of a specific metal gate integrated above the waveguide, that allows fine control of the conductance with high locality level. The paper highlights the linearity achievable in the conductance modulation, that can be exploited in a number of possible applications.

http://dx.doi.org/10.1364/ao.XX.XXXXXX

Silicon waveguides (WG) are not exclusively used to confine and transmit light by leveraging the difference of their refractive index with respect to the SiO_2 cladding and their extremely low absorption at near infrared telecom wavelengths. They are also a constituent part of a vast number of optoelectronic devices, like integrated photodetectors [1–3], thermal actuators [4], optical attenuators [5] and modulators [6], where the silicon core is also exploited as an electrically active element. For these devices, the density of free carriers in the WG becomes a fundamental parameter, as it directly determines their electrical behaviour. From an electrical point of view, a WG is a conductor with a conductivity $\sigma = q \cdot \mu \cdot p$ that depends on the carrier density p (usually defined by the doping level), q being the electronic charge and μ the mobility of the carriers in the Si crystal. Low-loss WGs in standard Silicon-On-Insulator (SOI) wafers usually show a native doping level around 10^{15} cm^{-3}, often p-type [7]. During fabrication, implantation of dopants can be exploited to change the electrical behaviour of a WG and create optoelectronic devices: doping levels around 10^{17} cm^{-3} are usually employed in modulators and heaters [8, 9], while extra selective doping as high as 10^{20} cm^{-3} is used to provide ohmic electrical contacts. However, what is not well established in literature is that these levels of doping do not always reflect in an equal amount of free carriers available for electronic conduction. Consequently, when measuring the electrical resistance of a WG or some of its optical properties, like propagation losses and refractive index, the obtained values can be very different from what expected from the doping level [10, 11]. This work specifically studies the effective free carriers density in silicon WGs, quantifying their real electrical conductance and its effects on the operation and design of electronic and photonic devices.

Figure 1 shows the two devices that were experimentally characterized in this work: a channel WG with 500 nm × 220 nm rectangular core, measured along its 100 µm longitudinal length (Fig. 1a) and a rib-shaped WG with 500 nm × 220 nm core, 900 nm × 90 nm slabs and 100 µm length, measured along its transversal dimension (Fig. 1b). Both devices were fabricated on the same chip in a commercial silicon photonic platform (Advanced Micro Foundry Pte Ltd, Singapore) with 10^{15} cm^{-3} p-type nominal doping and 10^{20} cm^{-3} p++ ohmic contacts, here labelled as Source (S) and Drain (D), to provide proper electrical connections. By knowing the geometrical size of the WGs (their length L and cross-section A) and assuming a carrier density equal to the doping level p, the geometrical resistance of the two structures can be computed as:

$$R = \frac{1}{q\,\mu\,p} \cdot \frac{L}{A} \tag{1}$$

For the considered geometries, values of about 113 MΩ and 28 kΩ are obtained for the channel and rib WG respectively, the latter being the sum of three regions (slab-core-slab) cascaded in series. Simulations of these geometries with the Sentaurus TCAD Software (Synopsys Inc., Mountain View, USA) confirm these values, which are reported in the I-V plots of Fig. 1c and 1d labelled as "Simulation without traps". In contrast, experimental results ("Experimental measurement" in the same figures) show that the current flowing in the WGs is orders of magnitude lower, thus revealing a much higher value of resistance.

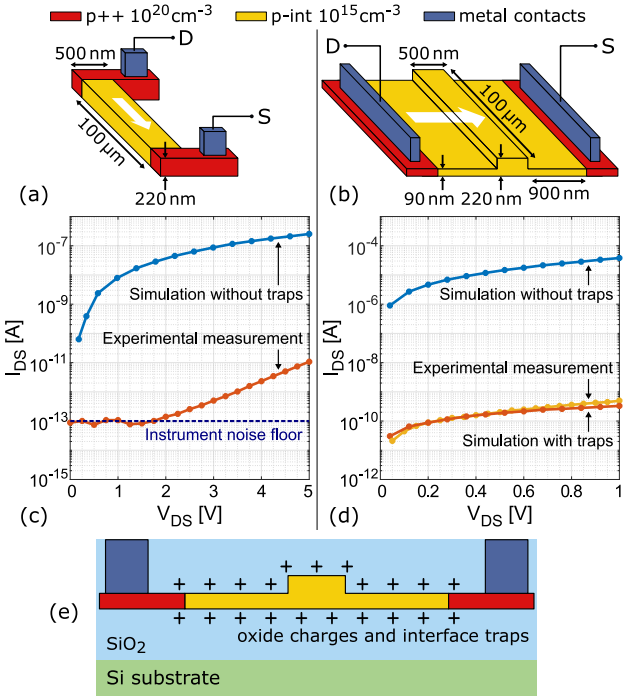

Fig. 1. (a), (b) Quoted sketches (not to scale) of the measured channel and rib WGs (longitudinal and transversal current flows respectively). (c) and (d) are the corresponding I-V curves, comparing the experimental measurements with the expected geometrical resistance (Simulation without traps) and with a simulation taking into account interface effects (Simulation with traps). Simulation parameters: 0.9×10^{11} cm^{-2} surface density of positive fixed charges, 1.1×10^{11} cm^{-2} rechargeable e-neutral traps at 0.8 eV and 1.1×10^{11} cm^{-2} h-neutral at 0.3 eV. SRH generation/recombination was also considered in the simulation. (e) WG cross section highlighting the presence of charges and traps at the interface between Si and SiO_2.

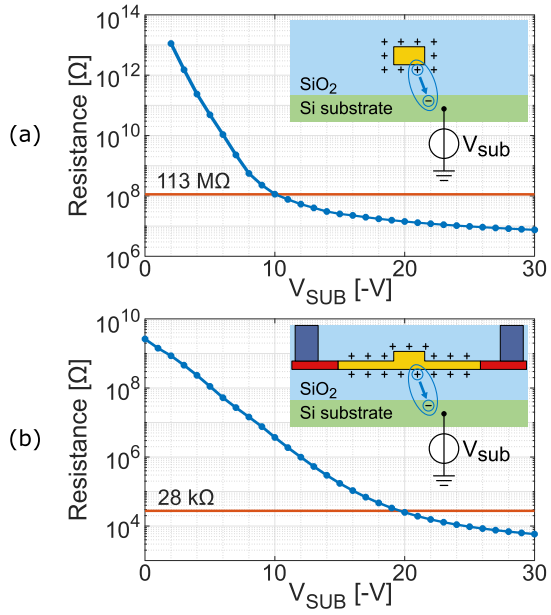

Fig. 2. Tuning of the waveguide resistance by means of the substrate negative voltage V_{sub} in channel (a) and rib (b) geometries. The insets qualitatively sketch the compensation of the positive Si/SiO_2 charges by the chip substrate at negative potential.

The huge discrepancy of about 5 orders of magnitude can be explained by considering the presence of charges and trap energy states at the Si/SiO_2 interface and inside the SiO_2 cladding, that originate during the chip production [12]. Figure 1e sketches the cross-section of the rib WG (the channel WG being simply the central part of the same) highlighting the presence and the role of these charges and traps. The holes initially available in the WG due to doping are electrostatically pushed towards the contacts by the oxide charges (predominantly positive in a Si/SiO_2 technology [12, 13]) or immobilized and removed from conduction by the interface traps, eventually depleting the core from free carriers. This effect is similar to what encountered in silicon nanowires [14] and nanomembranes [15] and more in general in devices with large surface-to-volume ratio, where depletion might occur to completion. The simulated I-V curve of Fig. 1d labelled as "Simulation with traps" confirms this behaviour. Here we used a density of charges and traps that is commonly reported in literature for SOI technology [12, 15] (relevant simulation parameters are listed in Fig. 1 caption). Numerical results match very well the experimental measurements, certifying that a standard SOI photonic technology produces native waveguides that are naturally almost fully depleted of carriers and consequently show a resistance many orders of magnitude higher than what expected. This is an important experimental evidence to be considered when designing photonic devices. As also reported in literature [10, 11, 15], this phenomenon strongly depends on the cladding material and on the thickness and doping level of the WG: highly doped devices, as 10^{17} cm^{-3} in [2], do not reach complete depletion, as it will be also demonstrated in the following.

The depletion of free-carriers in the WG can be externally controlled. Indeed, the effect of interface charges and traps can be counter-acted by diverting their electric field lines away from the WG towards a secondary electrode, as qualitatively sketched in the insets of Fig. 2. To this aim, the substrate of the chip can be effectively used, as its large size ensures high conductivity even with 10^{15} cm^{-3} doping. By applying a negative substrate voltage V_{sub} with respect to the D and S contacts, the interface effects can be counter-acted and the number of free carriers in the waveguide can be changed. The experimental dependence of the WG resistance as a function of the substrate voltage is shown in Fig. 2 for the channel (a) and rib (b) geometries. The resistance was calculated with a Keithley 4200-SCS source-measure unit (SMU) by measuring the current I_{DS} in the WG when applying $V_{DS} = 1$ V and a substrate voltage V_{sub} ranging from 0 V to -30 V. The experimental curves demonstrate that the resistance can be effectively modified from the very high initial state (when $V_{sub} = 0$) back to the "geometrical" value (full compensation of the interface effects) indicated by the horizontal line. The WG can be also driven into accumulation (holes concentration higher than the one defined by the doping) by further increasing V_{sub}, obtaining a resistance lower than the geometrical one. Both results of Fig. 2 show that an overall resistance variation larger than 5 orders of magnitude can be obtained with a 30 V substrate voltage span. Such a high tuneability range cannot be explained with a change in the carriers mobility and thus confirms that the substrate potential controls the number of available free carriers in the devices.

The importance of the substrate voltage in defining the type and concentration of carriers in a WG can be further appreciated in Fig. 3a. In this case we have designed a rib device with the same geometry as in Fig. 1b but with n++ contacts on the sides (10^{20} cm^{-3} doping) to obtain a rectifying behaviour instead of

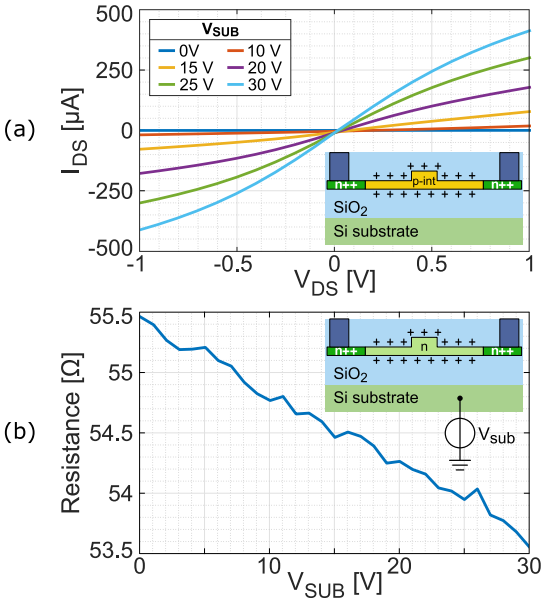

Fig. 3. (a) I-V curves of a n++-p-n++ structure for different voltages of the substrate. When a positive V_{sub} is applied, inversion occurs in the WG and current can flow between the D and S contacts. (b) Resistance tuning of a 2×10^{17} cm^{-3} n-doped waveguide. The high doping level prevents full depletion of the core and the substrate potential thus has a negligible effect.

an ohmic one. As it is, no current can flow in this n-p-n structure except for the one due to the reverse biased p-n junction. The experimental results show instead that when the substrate is positively biased so as to electrostatically induce electrons in the central p-type region, the core of the WG can be driven into inversion, passing from the initial prevalence of holes given by the p-type doping to a final prevalence of electrons induced by the substrate [16]. When this occurs, a current modulated by the substrate potential can flow in the device when applying a V_{DS} voltage to the contacts, demonstrating the effectiveness of the carriers control that can be obtained.

The same experiment was repeated also in a similar device with n++ contacts and 2×10^{17}cm^{-3} n-doped core (Fig.3b). This kind of structure is commonly embedded in photonic chips to create waveguide integrated heaters and in-line semi-transparent photodetectors [2, 4]. By comparing the number of traps at the interface, computed by considering the parameters of our simulation, with the number of available free carriers in the device (5×10^5 traps, 5×10^6 electrons), it is possible to predict that the depletion of the core does not happen in this case and that the substrate potential has a negligible effect. This is indeed confirmed by the experimental measurements, showing that the waveguide resistance is in very good agreement with the geometrical calculation (about 54 Ω) and that the same 30 V substrate voltage span employed in the previous experiments induces in this case only a 4% variation of the core resistance.

All these findings drive the attention to the role of the substrate of a silicon photonic chip, whose voltage should not be unintentionally left floating or grounded but should be set to a precise value in order to control the electronic properties of the devices integrated over it. When properly managed, this very important aspect can be exploited to obtain innovative functionalities from standard photonic devices, as in the following.

Figure 4a shows a micro-ring resonator of 20 μm radius where a device as the one of Fig. 1b was embedded, to be used as a thermal actuator. Recalling that the power dissipated by a heater with resistance R can be written as:

$$P = V_{DS} \cdot I_{DS} = \frac{V_{DS}^2}{R} = V_{DS}^2 \cdot G \qquad (2)$$

this actuator can be operated either by tuning its conductance $G = 1/R$ with the substrate potential V_{sub} or by changing the V_{DS} voltage applied across it. Figure 4b shows the experimental wavelength shift of the microring resonance, when the actuator is biased at a fixed voltage $V_{DS} = 16$ V and only the substrate potential is changed from $V_{sub} = 0$ V to $V_{sub} = -50$ V. A linear behaviour is observed, quantitatively appreciated also in Fig. 4c where the resonance peaks are plotted as a function of V_{sub}. This experimental result suggests that the substrate potential can induce a linear change of free carriers in the core and a consequent linear variation of the WG conductance G. The power dissipated by the actuator can be thus written as:

$$P = V_{DS}^2 \cdot G = V_{DS}^2 \cdot k \cdot |V_{sub}| \qquad (3)$$

where k is a parameter that linearly links the WG conductance to the substrate potential. In contrast, in a conventional heater

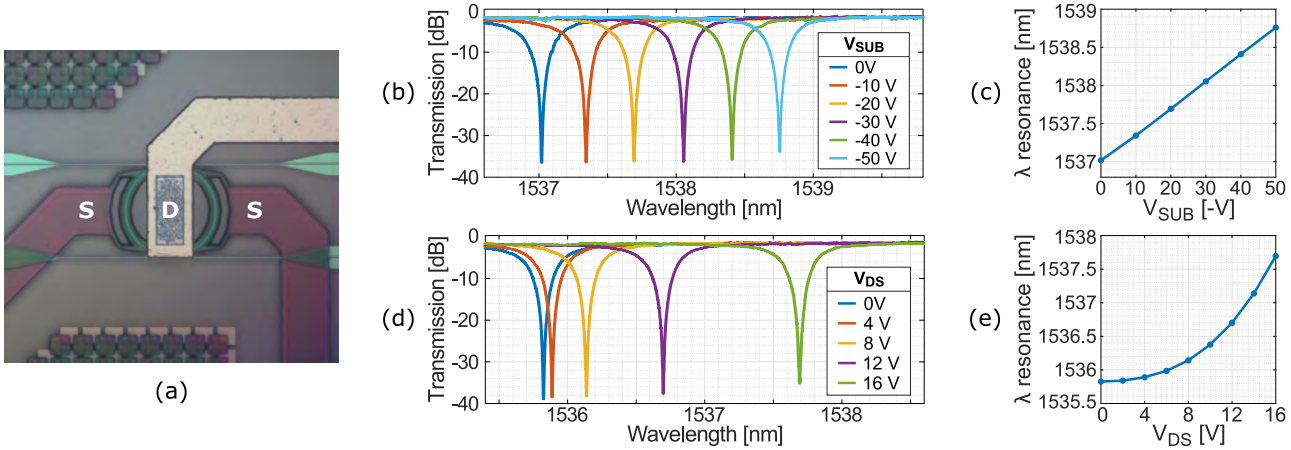

Fig. 4. (a) Photograph of a 20 μm radius micro-ring resonator with an embedded thermal actuator made as in Fig. 1b. (b) Tuning of the ring resonance by means of the substrate voltage when V_{DS} is fixed to 16 V and (c) corresponding plot of the resonant wavelength as a function of V_{sub}, showing a highly linear control. As a comparison, the resonance tuning when the actuator is operated in a standard way by changing the V_{DS} voltage across it is reported (d), (e), showing the expected quadratic behaviour.

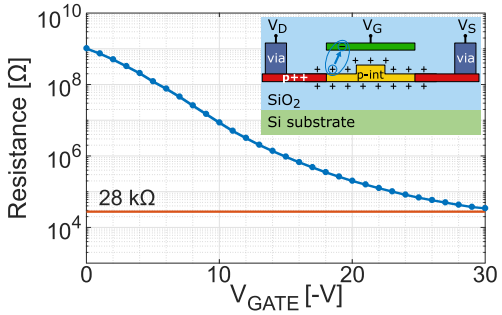

Fig. 5. Tuning of the WG resistance by means of a local gate electrode integrated over the core and biased at negative voltage to compensate the effect of the positive Si/SiO_2 charges. Full recovery of the carrier concentration to the doping level is experimentally demonstrated in a specific site of the photonic chip.

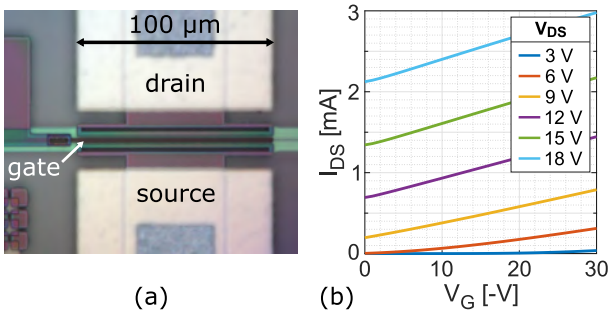

Fig. 6. (a) Microphotograph of a MOSheater prototype, where the electrical power is given by a fixed supply voltage between Source and Drain and the device conductance is changed by an independent Gate voltage. (b) Measured current I_{DS} in the MOSheater as a function of the gate voltage V_G for different V_{DS}, showing a linear dependence.

the conductance G is constant (apart from temperature-induced variations of the conductivity) and the dissipated power can only be changed quadratically by modifying the applied V_{DS} voltage. We have experimentally verified this situation on the same device by setting a fixed substrate potential $V_{sub} = -20\,\text{V}$ and by changing the voltage across the device from $V_{DS} = 0\,\text{V}$ to $V_{DS} = 16\,\text{V}$. Figure 4d shows the spectral shift of the resonance in this case, whose peak positions are summarized in Fig. 4e, showing the expected quadratic behaviour.

When the conductance of more than one device is to be controlled independently, the substrate potential cannot be used, as it is common to all the chip. Instead, the carrier concentration in a specific site of a complex photonic chip can be locally modified by means of a Gate (G) electrode integrated over the WGs. The inset of Figure 5 shows the schematic cross-section of the same rib device of Fig. 1b with the addition of a metal gate, integrated 700 nm above the core. The gate, fabricated with the metal layer closest to the WG, locally induces the same charge-control effect previously described, by diverting the electrostatic field of the Si/SiO_2 charges away from the core, allowing to control the carrier concentration. The experimental result shown in Figure 5 confirms that, by applying a voltage to the gate in the range from $V_G = 0\,\text{V}$ to $V_G = -30\,\text{V}$, the WG resistance can be varied in an interval of 5 orders of magnitude and restored to the expected value, in a similar way as with the substrate.

The possibility of locally modifying the waveguide conductance suggests the concept of a MOSheater (Fig. 6a), a linear thermal actuator where the power is provided by a fixed V_{DS} voltage applied between the Source and Drain contacts and the conductivity is linearly controlled, as given by Eq. 3, by a Gate electrode. Fig. 6b shows the current I_{DS} measured in a 100 µm long MOSheater as a function of the gate voltage V_G, for different values of V_{DS}. The measurements indicate that an heating power of about 10 mW, suitable for tuning photonic devices, can be obtained with V_{DS} around 10 V and a gate potential $V_G = -10\,\text{V}$. Notice that current can flow in the actuator even at $V_G = 0\,\text{V}$ when a sufficiently high V_{DS} voltage is applied, as in these conditions injection of carriers happens from the contacts and lowers the very high initial resistance of the core. The linearity in the power control of the MOSheater, here achieved for $V_{DS} > 8\,\text{V}$, is very beneficial, as it can reduce the complexity of the control algorithms for photonic devices. In addition, another advantage of this actuator is the zero static power required to control the gate and consequently the current in the device. This lowers the complexity of the external electronics, that now require a single driver stage shared among the drains of all the MOSheaters to provide the electrical power and very simple low-power control stages to drive the independent gates. A further optimization of the MOSheater with respect to our prototype can reduce to less than 10 V its operating voltages, making it compatible with standard electronic technologies. The active width of the device can be for example significantly increased with an interdigitated geometry, allowing to drive a larger current with reduced voltages.

Funding. EU project NEBULA in H2020-ICT-2019-2 under contract n. 871658.

Disclosures. The authors declare no conflicts of interest.

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