ANTIDERIVATIVE ANTIALIASING IN NONLINEAR WAVE DIGITAL FILTERS

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ABSTRACT

A major problem in the emulation of discrete-time nonlinear systems, such as those encountered in Virtual Analog modeling, is aliasing distortion. A trivial approach to reduce aliasing is oversampling. However, this solution may be too computationally demanding for real-time applications. More advanced techniques to suppress aliased components are arbitrary-order Antiderivative Antialiasing (ADAA) methods that approximate the reference nonlinear function using a combination of its antiderivatives of different orders. While in its original formulation it is applied only to memoryless systems, recently, the applicability of first-order ADAA has been extended to stateful systems employing their state-space description. This paper presents an alternative formulation that successfully applies arbitrary-order ADAA methods to Wave Digital Filter models of dynamic circuits with one nonlinear element. It is shown that the proposed approach allows us to design ADAA models of the nonlinear elements in a fully local and modular fashion, independently of the considered reference circuit. Further peculiar features of the proposed approach, along with two examples of applications, are discussed.

1. INTRODUCTION

In the recent years, much work has been done to develop faithful and computationally lightweight Virtual Analog models of nonlinear audio circuits [1–8]. Several techniques have been developed for the digital emulation of analog synthesizers [9–11], distortion pedals [12] and audio amplifiers [13, 14], that contain nonlinear circuit elements such as diodes [15–19], transformers [20], transistors [21] and tubes [22]. A major problem in Virtual Analog modeling is that nonlinear digital signal processing could potentially generate aliasing distortion in the output signals. This issue occurs when a band-limited input signal is processed by a nonlinear function, which may add to the signal spectrum additional frequency components that overcome the Nyquist frequency and are mirrored into the signal base-band as distortion artifacts, causing inharmonicity, beating, and heterodyning [23].

Aliasing could trivially be attenuated by using high oversampling factors, however, in real-time audio applications, this may be undesirable due to the large number of operations that need to be carried out by the CPU. Therefore, alternative, less expensive, antialiasing methods have been proposed for the implementation of oscillators for subtractive synthesis [23] and for the emulation of clipping stages employed in overdrive and distortion circuits [24, 25].

A further approach to reduce aliasing, with a broad applicability to a large class of nonlinear functions, called Antiderivative Antialiasing (ADAA), has been introduced by Parker *et al.* in [26] and is based on approximating the input signal as a continuous-time piecewise linear function, applying the nonlinear function to it, and convolving the resulting signal with the continuous-time impulse response of a lowpass filter, before sampling it back to the digital domain. This process leads to an approximation of the nonlinearity in terms of its antiderivatives, which introduces less aliasing. In [26], however, just first and second-order approximations based on antiderivatives are discussed. Successively, Bilbao *et al.* in [27] extended the method employing higher-order antiderivatives, reframing the approach as the repeated differentiation of a pth-order antiderivative of the nonlinear function. As two major flaws, ADAA presents a low-pass filtering effect and the introduction of a fractional delay of $p/2$ samples [28]. The first limitation can be easily overcome through mild oversampling, or by designing a simple linear filter. The additional introduced delay, however, becomes problematic in systems having feedback paths. For this reason, ADAA has been applied almost exclusively to memoryless systems [26,27,29]. An extension to stateful systems has been proposed by Holters in [30], and consists of a global parameter modification to the coefficient matrices of the state-space formulation, to compensate for the additional delay introduced in the system by the ADAA filter.

Inspired by the approach in [30], this paper presents a different methodology for applying pth order ADAA to stateful Wave Digital Filters (WDFs) with one nonlinearity. Such a methodology allows us to exploit the inherent modularity property of WDFs in the design of ADAA algorithms for Virtual Analog modeling. Section 2 briefly revises the main properties of WDFs with one nonlinearity such as their tree-like structure. Section 3 proposes a novel method to integrate first-order ADAA [26] into WDFs with one nonlinear element, while Section 4 generalizes the method to higher-order ADAA. Section 5 presents explicit Wave Digital (WD) exponential diode models suitable for first-order and second-order ADAA and characterized by analytical expressions employing the Lambert function. Such models are then extended for accommodating pairs of diodes in antiparallel in an explicit fashion. The presented models are then tested in the examples of application discussed in Section 6. Section 7 concludes this paper and proposes possible future developments.

2. BRIEF OVERVIEW OF WDF MODELING

WDF theory was first introduced by A. Fetteweis in the 1970s and later reorganized in [31], as an efficient technique to model analog reference circuits as digital filters, based on networks of input-output blocks characterized by scattering relations and communicating through port connections. In particular, a WDF is a port-wise lumped model of a reference circuit that detaches the topological information from the models of circuit elements. The reference topology is described through scattering junctions, called *adaptors*, enforcing Kirchhoff continuity laws, while circuit elements are derived from the lumped discretization of their constitutive equations. A peculiarity of WDFs is the use of the so-called *wave variables*, defined at one port of a circuit element as

$$a = v + Zi \qquad b = v - Zi \tag{1}$$

where v is the port voltage, i is the port current, a is the wave incident to the element, b is the wave reflected from the element and Z is an additional free parameter, called *reference port resistance*. This free parameter is set to *adapt* linear circuit elements, thus obtaining explicit WD scattering relations in the discrete-time domain in which the reflected wave does not depend on the incident wave. In this way, local delay-free loops arising from the port connections of elements to WD junctions are eliminated. In particular, dynamic elements (i.e., capacitors and inductors) implemented with the trapezoidal discretization rule, when adapted, are realized through mere one-sample delays. Constitutive equations in the continuous-time Kirchhoff domain, discrete-time scattering relations in the WD domain and the corresponding adaptation conditions for the most common linear one-port elements are reported in Table 1. V_g, R, C and L indicate a voltage source E_g with internal series resistance R_g, a resistor, a capacitor and an inductor, respectively. On the other hand, connection networks embedding the

Table 1: *Wave mapping of common WD linear one-port elements.*

	Constit. eq.	Wave mapping	Adapt. cond.
V_g	$v = E_g + R_g i$	$b[k] = E_g[k]$	$Z = R_g$
R	$v = Ri$	$b[k] = 0$	$Z = R$
C	$i(t) = C\frac{dv(t)}{dt}$	$b[k] = a[k-1]$	$Z = \frac{T_s}{2C}$
L	$v(t) = L\frac{di(t)}{dt}$	$b[k] = -a[k-1]$	$Z = \frac{2L}{T_s}$

topological information of the reference circuits are implemented in the WD domain using scattering junctions characterized by scattering matrices, and called *adaptors* [31] in WDF theory. General formulas for computing the scattering matrix of arbitrary reciprocal or nonreciprocal connection networks in the WD domain are discussed in [32–35].

2.1. WDFs as Connection Trees

In order to ensure the computability of a WD structure, the corresponding signal-flow diagram should not contain any delay-free loop [31, 36, 37]. Sarti *et al.* [38] proposed a systematic method to implement WD structures that can accommodate up to one nonlinear element in an explicit fashion, i.e., without using iterative solvers, and showed that computability is guaranteed if the network of adaptors has a tree-like structure without delay-free-loops. The result is the so-called *Binary Connection Tree* (BCT), which has one (nonlinear) element as *root*, an interconnection of series/parallel 3-port scattering junctions as *nodes*, and linear one-port elements as *leaves*. Moreover, each WD junction is adapted towards the root, which means that ports of junctions connected to other junctions (i.e., other nodes) and the one connected to the nonlinear element (i.e., the root) are all made reflection free, by properly setting the free parameters at those ports.

In the light of the recent advances in the WD modeling of reciprocal [35] and non-reciprocal [34] junctions, the BCT concept can be easily generalized to the concept of *Connection Tree* (CT), whose root is a one-port nonlinear element, nodes can be N-port adaptors with $N \geq 3$ and leaves are linear elements. Under the assumption that no delay-free-loops are present, also a CT can be implemented in an explicit fashion.

The evaluation of a CT consists of three main phases. At first, the *forward scan* phase is performed. It consists of traversing the CT from the leaves to the root. At each sample k, the waves reflected from adapted linear one-port elements are given by the simple scattering relations reported in Table 1. Therefore it is possible to compute all the waves reflected from the junctions at their adapted ports, performing the scattering operations in the correct order (i.e., the computational flow goes from the leaves to the root). The second phase consists of the *local nonlinear scattering stage* at the root element, which outputs the wave incident to the adjacent adaptor. Lastly, the *backward scan* stage consists of traversing the tree structure from the root to the leaves, updating the waves incident to all the one-port elements.

3. FIRST-ORDER ANTIDERIVATIVE ANTIALIASING IN NONLINEAR WDF

Let us consider the generic WDF in Fig. 1 characterized by a single (reciprocal or nonreciprocal) N-port WD junction. $N-1$ linear one-ports and one nonlinear element are connected to the junction. Since WDF in Fig. 1 has a CT structure (i.e., the nonlinear element is the root, the linear elements are the leaves and the node is the N-port junction), it can be implemented in an explicit fashion using the procedure, based on forward scan, local nonlinear scattering and backward scan, discussed in the previous Section. Depending on the reference circuit the single node can be decomposed into an interconnections of nodes without delay-free-loops (e.g., other CTs with multiple nodes or BCTs). However, it is worth noticing that we do not lose generality by describing the topological information with a single node. The scattering matrix $\mathbf{S}$ characterizing the (reciprocal or nonreciprocal) WD junction can be computed according to the formulas presented in [34, 35] and given the N free parameters $Z_1, \ldots, Z_N$. The port of the WD junction facing the nonlinear element is made reflection free by choosing the free parameter at that port in such a way that the corresponding diagonal entry of the scattering matrix $\mathbf{S}$ goes to zero.

Matrix $\mathbf{S}$ relates incident and reflected waves at a sampling time step k as

$$\mathbf{a}[k] = \mathbf{S}\mathbf{b}[k], \tag{2}$$

Waves incident to the elements are collected into the column vector $\mathbf{a}[k] = [a_1[k], \ldots, a_N[k]]^T$. We assume, that the WD one-port elements are ordered as follows. Waves $a_1[k], \ldots, a_M[k]$ are incident to M dynamic elements (e.g., capacitors or inductors) with $M < N$. The wave at position $M+1$ of vector $\mathbf{a}[k]$, called $a_\xi[k]$, is incident to the nonlinear element. Finally, waves $a_{M+2}[k], \ldots, a_N[k]$ are incident to linear instantaneous elements

(e.g., resistors or resistive sources). Therefore, vector $\mathbf{a}[k]$ can be expressed as

$$\mathbf{a}[k] = [a_1[k], \dots, a_M[k], a_\xi[k], a_{M+2}[k], \dots a_N[k]]^T.$$

Similarly we can define the vector $\mathbf{b}[k]$ as the column vector of waves reflected from the elements and incident to the WD junction. Waves reflected from linear elements are computed according to Table 1, while the nonlinear element at the root is characterized by the scattering relation $b = f(a)$.

Let us now locally apply the first-order ADAA method proposed in [26] to the nonlinear scattering relation $b = f(a)$, by substituting f with the approximation

$$\tilde{f}(a[k], a[k-1]) = \begin{cases} \frac{F_1(a[k]) - F_1(a[k-1])}{a[k] - a[k-1]} & \text{if} \quad a[k] \not\approx a[k-1] \\ f\left(\frac{a[k]+a[k-1]}{2}\right) & \text{if} \quad a[k] \approx a[k-1] \end{cases} \tag{3}$$

where $a[k]$ and $b[k]$ are the discrete-time wave signals and F_1 is the first-order antiderivative of f.

Unfortunately, as outlined in [26, 30], the first-order ADAA filter introduces half-sample delay in the digital structure, altering the temporization of the system. In particular, at each time-step k, the non-antialiased version of the same system would have a unitary delay that temporarily stores the state, to be used at time-step $k+1$. However, the additional delay introduced by ADAA in the feedback path sums up to the unitary delays implementing capacitors and inductors, while causing the total delay to become 1.5-samples long. In addition to the altered temporization of the system, ADAA introduces a misalignment in time between the signals entering the WD junction with scattering matrix $\mathbf{S}$ during the backward scan stage.

Let us consider (2) as the generic scattering operation, at time step k, performed throughout the backward scan stage. The column vector $\mathbf{b}[k]$ of waves reflected from the elements and incident to the WD junction is given by

$$\mathbf{b}[k] = [b_1[k], \dots, b_M[k], \tilde{b}_\xi[k], b_{M+2}[k], \dots, b_N[k]]^T \ ,$$

where, in turn, $\tilde{b}_\xi[k]$ is defined as

$$\tilde{b}_\xi[k] = \tilde{f}(a_\xi[k], a_\xi[k-1]) \ . \tag{4}$$

Since $\tilde{f}$ introduces a half sample delay, it becomes clear that there is a misalignment in time between $\tilde{b}_\xi[k]$ and all the other elements of $\mathbf{b}[k]$. To synchronize the signals, we apply a half-sample delay filter with Z-domain transfer function $H(z) = \frac{1}{2}(1 + z^{-1})$ to all the entries in $\mathbf{b}[k]$ but $\tilde{b}_\xi[k]$. It is worthwhile noticing that such a filter $H(z)$ acts as the ADAA filter (3) in the linear case; hence, to some extent, we are applying the same antialiasing filter even to the linear elements of the system. Thus, we obtain a synchronized version of (2), expressed as

$$\tilde{\mathbf{a}}[k] = \mathbf{S}\tilde{\mathbf{b}}[k] \tag{5}$$

where $\tilde{\mathbf{b}}[k] = [\tilde{b}_1[k], \dots, \tilde{b}_M[k], \tilde{b}_\xi[k], \tilde{b}_{M+2}[k], \dots, \tilde{b}_N[k]]^T$ and

$$\tilde{b}_n[k] = \frac{1}{2}(b_n[k] + b_n[k-1]) \quad \text{with} \quad 1 \le n \le N \quad \wedge \quad n \neq \xi. \tag{6}$$

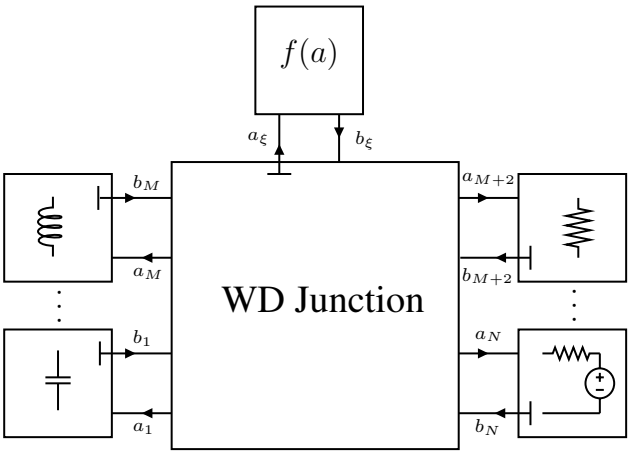

Figure 1: Single-junction WDF with one nonlinear element.

The half-sample delay filter applied to each entry of $\mathbf{b}[k]$, with the exception of $\tilde{b}_\xi[k]$, resolves the issue of time misalignment between the waves incident to the WD junction during the backward scan. The last open problem to be addressed is the altered timing due to the added delay. If we further expand (5), considering the waves reflected from dynamic elements, according to Table 1, we obtain

$$\tilde{\mathbf{b}}[k] = [\pm\tilde{a}_1[k-1], \dots, \pm\tilde{a}_M[k-1], \tilde{b}_\xi[k], \tilde{b}_{M+2}[k], \dots, \tilde{b}_N[k]]^T \tag{7}$$

where $\tilde{a}_n[k-1] = \frac{1}{2}(a_n[k-1] + a_n[k-2])$.

Equation (7) puts in evidence that the introduced half sample delay results in a 1.5-samples total delay in the feedback path of the system. The additional delay is compensated employing a similar method to that described in [30] for state-space representations. Since the coefficient in $\mathbf{S}$ depends on the sampling period T_s, we can modify them for the "expanded" sampling period $\tilde{T}_s = 1.5T_s$, by noticing that a 1.5 samples delay corresponds to a one sample delay at the reduced sampling frequency of $\tilde{f}_s = 2f_s/3$. Thus, (2) is approximated with

$$\mathbf{a}[k] \approx \tilde{\mathbf{S}}\tilde{\mathbf{b}}[k], \tag{8}$$

where $\tilde{\mathbf{b}}[k]$ represents the vector $\mathbf{b}[k]$ after the application of the synchronization delays in (5) and (6). Matrix $\tilde{\mathbf{S}}$ is defined as $\tilde{\mathbf{S}} = \mathbf{S}(\tilde{T}_s)$, which means that the free parameters $Z_1, \dots, Z_N$ essential for the computation of the scattering matrix need to be changed according to the expanded sampling period $\tilde{T}_s$. In particular, for capacitors we set $Z_n = \tilde{T}_s/(2C_n)$ and for inductors $Z_n = 2L_n/\tilde{T}_s$. Finally, operating the system at its original sampling frequency f_s, but with modified coefficients, allows us to compensate for the additional delay, resulting in the adaptation of the ADAA method to nonlinear stateful WDFs.

The implementation procedure is resumed in the following pseudo-code snippet, considering an input signal $V_{\text{in}}[k]$ coming from a voltage source connected to the jth port of the WD junction. Let us assume that the output signal is the port-voltage $V_{\text{out}}[k]$ at the lth port. Moreover, we define $\mathbf{s}_\xi$ as the ξth row vector of matrix $\tilde{\mathbf{S}}$.

Algorithm 1 ADAA in One-Junction WDFs

1 **for** k=1:length(V_{in}) **do**
2 $b_1[k], \dots, b_M[k] \leftarrow \pm a_1[k-1], \dots, \pm a_M[k-1]$
3 $b_j[k] \leftarrow V_{\text{in}}[k] \quad M+2 \leq j \leq N$ ▷ Input Signal
4 $\mathbf{b}[k] = [b_1[k], \dots, b_M[k], 0, b_{M+2}[k], \dots, b_N[k]]^T$
5 $a_\xi[k] \leftarrow \tilde{\mathbf{s}}_\xi \mathbf{b}[k]$ ▷ Forward Scan
6 $\tilde{b}_\xi[k] \leftarrow \tilde{f}(a_\xi[k], a_\xi[k-1])$ ▷ 1st-order ADAA
7 $\tilde{b}_n[k] \leftarrow \frac{1}{2}(b_n[k] + b_n[k-1]) \quad n \neq \xi$
8 $\tilde{\mathbf{b}}[k] = [\tilde{b}_1[k], \dots, \tilde{b}_M[k], \tilde{b}_\xi[k], \tilde{b}_{M-2}[k], \dots, \tilde{b}_N[k]]^T$
9 $\mathbf{a}[k] \leftarrow \tilde{\mathbf{S}}\tilde{\mathbf{b}}[k]$ ▷ Backward Scan
10 $\tilde{a}_l[k] = \frac{1}{2}(a_l[k] + a_l[k-1])$
11 $V_{\text{out}}[k] \leftarrow \frac{1}{2}(\tilde{a}_l[k] + \tilde{b}_l[k])$ ▷ Output Signal
12 **end for**

In order to compute the output voltage V_{out}, the wave incident to the lth element needs to be aligned with its reflected wave, as shown in line 10 of Alg. 1.

4. HIGHER-ORDER ANTIDERIVATIVE ANTIALIASING IN NONLINEAR WDF

The approach described in Section 3 can be extended to higher-order ADAA methods, to obtain improved aliasing suppression. As before, we consider the same WDF of Fig. 1, with the difference that the nonlinear mapping f is substituted with a generic pth-order ADAA approximation. Thus, the wave reflected from the nonlinear element $\tilde{b}_\xi[k]$ is now defined as

$$\tilde{b}_\xi[k] = \tilde{f}(a_\xi[k], \dots, a_\xi[k-p]), \tag{9}$$

where $\tilde{f}(a_\xi[k], \dots, a_\xi[k-p])$ is the pth-order ADAA approximation of $b = f(a)$. In [26] a second-order ADAA method is provided, while an alternative general formulation for ADAA of arbitrary order p is presented in [27]. As an example, second-order ADAA proposed in [27] (i.e., $p = 2$) and applied to the reference function $f(a)$ yields

$$\tilde{f}(a[k], a[k-1], a[k-2]) = \frac{2}{a[k] - a[k-2]} \times \left(\frac{F_2(a[k]) - F_2(a[k-1])}{a[k] - a[k-1]} - \frac{F_2(a[k-1]) - F_2(a[k-2])}{a[k-1] - a[k-2]} \right), \tag{10}$$

where F_2 is the second-order antiderivative of f. For the treatment of numerical ill-conditioning of (10), possibly occurring when $a[k] \approx a[k-1]$, $a[k] \approx a[k-2]$ or $a[k-1] \approx a[k-2]$, the reader is referred to [27].

In pth-order ADAA, the approximation $\tilde{f}$ of f introduces a delay of $p/2$ samples [28], causing the waves incident to the junction in vector $\mathbf{b}[k]$ to be misaligned in time. Therefore, we need to apply synchronization delays, similarly to what done in (6). In particular, with higher-orders, the synchronization delays are fractional only when p is odd. For instance, if $p = 2$ all the signals entering the junction, but the wave reflected from the nonlinear element, have to be delayed by one sample. To synchronize the signals, let us introduce a (potentially) fractional delay of $p/2$ samples, with Z-domain transfer function $H_p(z)$. In this work, we use the delay filter defined below.

$$H_p(z) = \begin{cases} \frac{1}{2}\left(z^{-\lfloor \frac{p}{2} \rfloor} + z^{-(\lfloor \frac{p}{2} \rfloor + 1)}\right) & \text{if } p \text{ is odd} \\ z^{-p/2} & \text{if } p \text{ is even} \end{cases} \tag{11}$$

Other choices of delay filters are possible; however, it is advisable to use filters that are as spectrally flat as possible. If we define $B_n(z)$ as the Z-transform of the discrete-time wave signal incident to port n of the WD junction, i.e., $b_n[k]$, a synchronized signal $\tilde{B}_n(z)$ with $n \neq \xi$ is obtained by applying the filter $H_p(z)$,

$$\tilde{B}_n(z) = H_p(z) B_n(z) \quad \text{with} \quad n = 1, \dots, N \quad \wedge \quad n \neq \xi, \tag{12}$$

where $\tilde{B}_n(z)$ is the Z-transform of $\tilde{b}_n[k]$. A synchronized version of $\mathbf{b}[k]$ can now be defined as

$$\tilde{\mathbf{b}}[k] = [\tilde{b}_1[k], \dots, \tilde{b}_M[k], \tilde{b}_\xi[k], \tilde{b}_{M+2}[k], \dots, \tilde{b}_N[k]]^T.$$

However, as in the previous Section, we still need to compensate for the additional delay of $p/2$ samples introduced in the feedback path of the WDF by the pth-order ADAA method. Delay compensation is achieved by modifying the coefficients of the system according to the expanded sampling period $\tilde{T}_\text{s} = (1 + p/2)T_\text{s}$. In fact, a delay of $(1 + p/2)$ samples at the reduced sampling frequency $\tilde{f}_\text{s} = f_\text{s}/(1 + p/2)$ corresponds to a one-sample delay at the reference sampling frequency f_s. This translates to the use of a modified scattering junction $\tilde{\mathbf{S}} = \mathbf{S}(\tilde{T}_\text{s})$ in both the forward scan stage and in backward scan stage.

In the case of a multi-node CT structure, the procedure is analogous, having to adjust the coefficients for each junction according to the expanded sampling period $\tilde{T}_\text{s}$. We achieve signal synchronization during the backward scan by applying the $H_p(z)$ filter to waves incident to each junction, with the exception of waves incident to ports facing the nonlinear element or other junctions.

5. EXPLICIT WAVE DIGITAL ADAA MODELS OF DIODES BASED ON THE LAMBERT W FUNCTION

Nonlinear elements commonly encountered in Virtual Analog applications are often described through implicit functions, thus requiring iterative solvers (e.g., Newton-Raphson solvers) to run. However, the scattering behavior of a single exponential diode or a pair of exponential diodes in antiparallel can be expressed through explicit relations between the WD port variables by employing the Lambert W function, as discussed in [15, 17, 39]. This Section revises the aforementioned scattering relations and introduces first- and second-order antiderivatives of both wave mappings that can be employed in first- and second-order ADAA.

5.1. Single diode

Let us consider the large-signal Shockley diode model, which relates the current i through the exponential p-n junction to the voltage v across it

$$i = I_s \left(e^{\frac{v}{\eta V_t}} - 1 \right), \tag{13}$$

where I_s is the saturation current, V_t is the thermal voltage, and η is the ideality factor. The nonlinear equation (13) can be expressed

in the WD domain as an explicit mapping $b = f(a)$ [15, 17];

$$\begin{aligned} f(a) &= g(a, Z, Is, V_t, \eta) \\ &= a + 2ZI_s - 2\eta V_t \omega \left(\frac{a + ZI_s}{\eta V_t} + \log \left(\frac{ZI_s}{\eta V_t} \right) \right), \end{aligned} \tag{14}$$

where ω indicates the Omega Wright function, defined in terms of the principal branch of the Lambert function W_0 as $\omega(x) = \mathrm{W}_0(e^x)$ [39]. The first-order antiderivative of (14) is

$$F_1(a) = \frac{a^2}{2} + 2ZI_s a - \eta^2 V_t^2 \omega(\phi(a))(2 + \omega(\phi(a))), \tag{15}$$

while the second-order antiderivative reads as follows

$$F_2(a) = \frac{a^3}{6} + ZI_s a^2 - \frac{\eta^3 V_t^3}{6} \omega(\phi(a))(12 + 9\omega(\phi(a)) + 2\omega(\phi(a))^2) \tag{16}$$

where

$$\phi(a) = \frac{a + ZI_s}{\eta V_t} + \log \left(\frac{ZI_s}{\eta V_t} \right). \tag{17}$$

5.2. Pair of Diodes in Antiparallel

The hard clipping function commonly encountered in distortion and overdrive circuits [2, 15–17, 40] is often implemented through a pair of identical diodes in antiparallel. In the considered WD implementation they are modeled as a single nonlinear element whose $i - v$ characteristic is

$$i = I_s \left[\left(e^{\frac{v}{\eta V_t}} - 1 \right) - \left(e^{\frac{-v}{\eta V_t}} - 1 \right) \right]. \tag{18}$$

Assuming that only one of the two diodes is conducting at a given time instant [15, 17], the following nonlinear wave mapping for two identical antiparallel diodes can be formulated as

$$f(a) = \mathrm{sign}(a) g(|a|, Z, I_s, V_t, \eta), \tag{19}$$

where $\mathrm{sign}(a)$ is the sign function. The first-order antiderivative of (19) has been derived as

$$F_1(a) = \frac{a^2}{2} + 2ZI_s|a| - \eta^2 V_t^2 \omega(\phi(|a|)) \left(2 + \omega(\phi(|a|))\right). \tag{20}$$

The second-order antiderivative F_2 has been derived as

$$\begin{aligned} F_2(a) = &\frac{a^3}{6} + ZI_s \mathrm{sign}(a) a^2 - \frac{V_t^3 \eta^3 \mathrm{sign}(a)}{6} \times \\ &\omega(\phi(|a|))(12 + 9\omega(\phi(|a|)) + 2\omega(\phi(|a|))^2). \end{aligned} \tag{21}$$

Equations (14) and (19) with their antiderivatives can be reused to apply first- and second-order ADAA in WD structures describing different reference circuits containing diodes, due to the intrinsic modularity of WDFs.

6. EXAMPLES OF APPLICATION

In this section, we propose the application of the methods formalized in Section 3 and Section 4 to two Virtual Analog models that are characterized by a significant amount of aliasing distortion. The proposed WD implementations employ explicit nonlinear wave mappings based on the antiderivates derived in Section 5.

6.1. Diode Clipper

A large number of digital emulations of musical circuits that generate aliasing distortion employs clipping and limiting functions. This type of waveshaping is in fact common in guitar distortion and overdrive effects, and many different Virtual Analog implementations have been discussed in the literature [2, 15–17, 40]. A common circuit implementation of a clipping stage is the passive diode clipper shown in Fig. 2. This circuit, which consists of a RC net and two antiparallel diodes, is used to “clip" voltage signals whose amplitude exceed approximately ± 0.7 V.

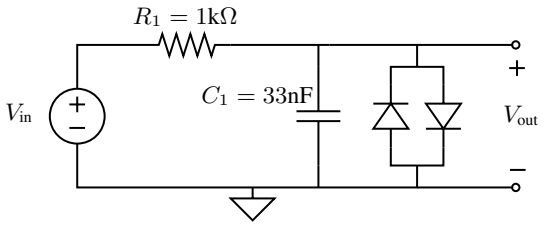

Figure 2: Circuit schematic of the Diode Clipper stage.

The implemented WDF is shown in Fig. 3. It consists of one series 3-port junction $\mathcal{S}_1$ and one parallel 3-port junction $\mathcal{P}_1$, and the input signal has been modeled through a voltage generator with internal series resistance $R_{\mathrm{in}} = 0.15\ \Omega$. The two antiparallel diodes are grouped together as one nonlinear element placed at the root of a BCT structure and characterized by the explicit relation (19). In particular, first-order ADAA is employed using (3) in conjunction with (20). Second-order ADAA, instead, uses (10) along with the first- and second-order antiderivatives (20) and (21). Moreover, care must be taken when numerical ill-conditioning occur, as specified in [27].

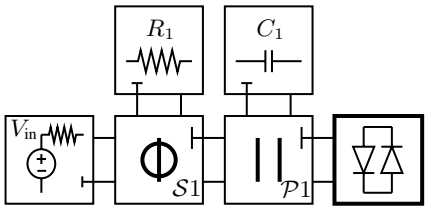

Figure 3: WDF implementation of the diode clipper.

The circuit has been tested with a sinusoidal input voltage $V_{\mathrm{in}}(t) = 10 \sin(2\pi f_0 t)$ with fundamental frequency $f_0 = 1244.5$ Hz, and reference sampling frequency $f_s = 44.1$ kHz. The magnitude spectra of the trivial implementation (i.e., without antialiasing) of the diode clipper circuit, as well as the versions with ADAA filters are illustrated in Fig. 4. Harmonic components are highlighted with an ‘x’, while all the other spikes in the spectrum correspond to aliased components. Fig. 4 shows how ADAA efficiently suppresses aliased components, especially at lower frequencies. However, it is worth recalling that high-frequency disturbances are often inaudible due to auditory masking effects. Moreover, results show that a $\times 2$ oversampling for the ADAA is sufficient to obtain suppression of aliased components comparable to non-antialiasied implementations with higher ($\times 6$) oversampling factors, especially employing the second-order ADAA method.

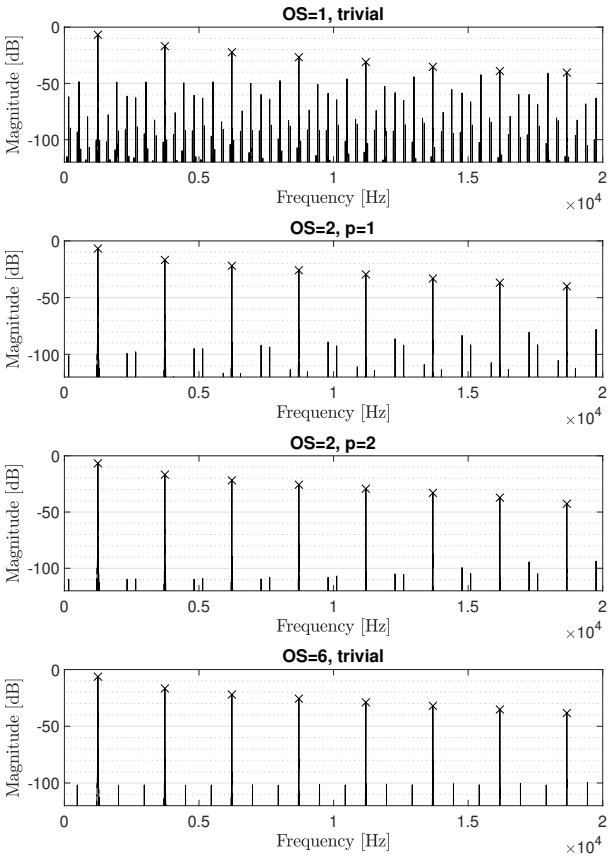

Figure 4: Diode clipper spectra employing different ADAA orders p and oversampling factors OS, with reference sampling frequency $f_s = 44.1$ kHz and a sinusoidal input at 1244.5 Hz, with amplitude of 10 V.

A possible metric to measure the suppression of the aliased components with respect to desired harmonic distortion components of the clipping stage is the Signal-to-Noise Ratio (SNR), here defined as a power ratio between desired harmonic components and aliased components. The performances have been evaluated by measuring the SNR for a set of sinusoidal inputs at different fundamental frequencies, ranging from 1 kHz to 10 kHz. The desired harmonic components are found by evaluating the model without any aliasing mitigation at a $\times 128$ oversampling factor. Those harmonics are then subtracted from the spectra of various simulations, with and without ADAA, at different oversampling factors, obtaining as residuals the aliased components. Finally, the ratio between the desired harmonics and the residuals is converted to the dB scale. Since in audio applications the SNR is only meaningful at audible frequencies, all signals were low-pass filtered to 18 kHz prior to the SNR evaluation. In figure 5, OS indicates the oversampling factor that multiplies the reference sampling frequency $f_s = 44100$ Hz, and p indicates the ADAA order; *trivial* refers to the output without any aliasing mitigation.

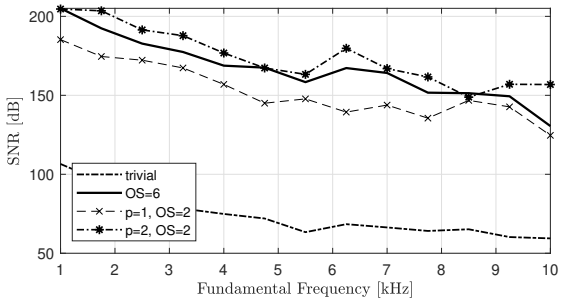

Figure 5: Diode clipper SNR.

6.2. Envelope Follower

The envelope follower is a circuit used to detect the amplitude variation of an input signal, extracting from it a smooth voltage signal that resembles its envelope, which may then be used to modify the input amplitude dynamics in terms of attack and release, or even to control other parameters. Its behaviour is governed by a single diode that rectifies the signal, followed by an RC filter that smooths rapid amplitude variations, creating the overall amplitude shape of the input signal. The reference circuit schematic is depicted in Fig. 6, while the corresponding WDF is shown in Fig. 7.

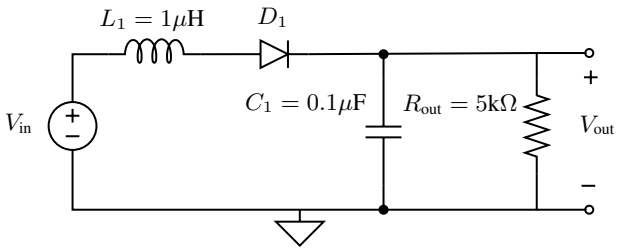

Figure 6: Envelope follower schematic.

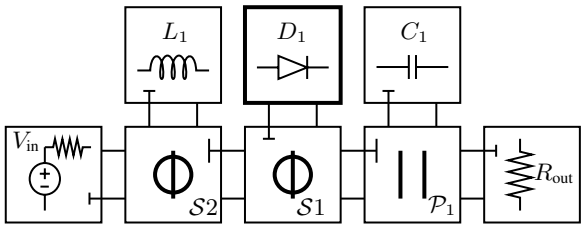

Figure 7: WDF Model of the envelope follower.

ADAA is implemented employing (3) and (10) in conjunction with the antiderivatives (15) and (16) of the single diode explicit model (14). Results obtained from different simulations are reported in Fig. 8. In particular, we show aliasing suppression per-

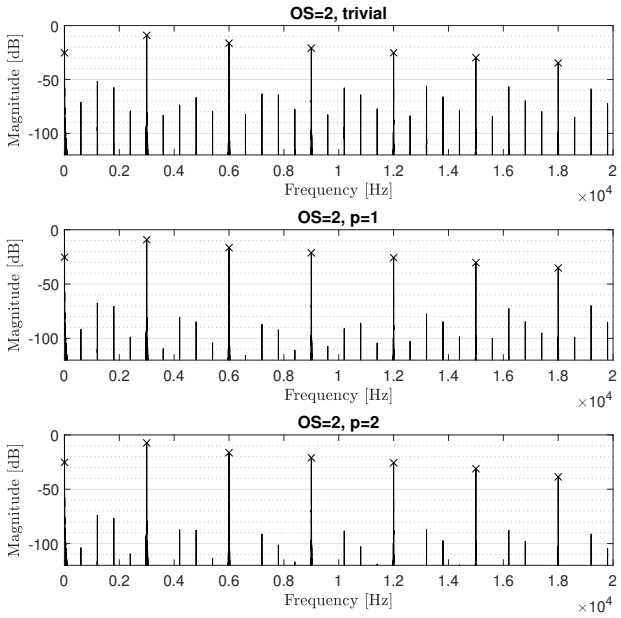

Figure 8: Envelope follower spectra employing different ADAA orders p and oversampling factors OS, with reference sampling frequency $F_s = 44.1$ kHz and a sinusoidal input at 3 kHz, with amplitude of 5V.

formances obtained employing first and second-order ADAA with an oversampling factor of 2.

7. CONCLUSIONS AND FUTURE WORK

In this paper, we showed how to integrate arbitrary-order ADAA methods into dynamic WDFs with one nonlinear element. The results show good aliasing suppression performances, even with low oversampling factors. It is worth noticing that the proposed approach for performing ADAA in the WD domain fully preserves the modularity properties of traditional WDFs. It is indeed straightforward to change/replace the WD model based on ADAA of the nonlinear element, with no need of redesigning the rest of the WD structure. On the other hand, once an ADAA-based WD model of a reference nonlinear element (e.g., diode or pair of diodes in antiparallel) has been derived it can be reused for implementing completely different circuits containing the same nonlinear element.

Moreover, the proposed approach allows us to implement dynamic circuits with one nonlinearity in a fully explicit fashion while performing aliasing reduction. This property is particularly appealing when it comes to develop Virtual Analog applications that need to run at real-time need with a low computational cost.

As a problem of ADAA filters, it is worth recalling that their response is not spectrally flat, and, in particular, their inherent low-pass filtering effect could be undesirable. Even if this effect could be easily compensated employing a linear filter, additional spectral shaping would be introduced when the method is applied to stateful systems. The remedy to such spectral shaping is mild oversampling, that limits the introduced distortion, while maintaining superior antialiasing performances [30].

As interesting future developments, we wish to extend the proposed ADAA approach to WD structures with multiple nonlinearities, while maintaining the aforementioned modularity properties as much as possible [18, 41–43]. Another compelling development would be to generalize ADAA techniques such that they can be applied to nonlinear blocks with multiple inputs, e.g., employing ADAA for modeling multi-port nonlinearities like transistors or vacuum tubes [21, 42].

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