Fault-tolerant Control of CPS-PWM Based Cascaded Multilevel Inverter with Faulty Units

Liansong Xiong, *Member, IEEE,* Fang Zhuo, *Member, IEEE,* Xiaokang Liu, Zhao Xu, *Senior Member, IEEE,* and Yixin Zhu, *Member, IEEE*

***Abstract*—Bypassing the faulty power unit(s) of the regenerative cascaded multilevel inverter (CMI) directly results in a series of adverse influences. The existing solutions are not easy to implement and only effective for the Y-connected devices composed of regenerative CMIs. To bypass the faulty power units seamlessly, the corresponding control strategies must guarantee 1) constant equivalent switching frequency, 2) constant sampling frequency and 3) constant fundamental voltage amplitude. To this end, a generic fault-tolerant control strategy, which 1) adjusts the carrier frequency and 2) simultaneously changes the CMI DC voltage and/or the modulation ratio, is presented in this paper. It is applicable for the device composed of Carrier Phase Shifting PWM (CPS-PWM) based CMIs to ride through faults seamlessly, whether it is a single-phase system, a three-phase system (be it Δ-connected or Y-connected) or a multi-phase system. The detailed implementation is also analyzed by modeling the output voltage of the CPS-PWM based CMI. The experimental results verify the validity and superiority of the proposed fault-tolerant strategy for the CPS-PWM based CMI system with faulty power units.**

***Index Terms*—Regenerative CMI, STATCOM, Faulty power units, Fault-tolerant control, Carrier phase shifting PWM.**

I. Introduction

CASCADED multilevel inverter (CMI) possesses many excellent merits such as high voltage operating capability, reduced voltage harmonics, increased efficiency and modularized system configuration [1,2]. Therefore, it has recently become an attractive solution for high-voltage applications such as variable-frequency drive [3-5], static synchronous compensators (STATCOM) [6-8] and energy storage systems [9-10]. However, a large number of power switches and electrical components are always required in these high-voltage converters consisting of CMIs, which will dramatically weaken the system stability and reliability [11-14]. One power unit fault may result in serious failures of the whole CMI based system [14-18]. In this sense, these systems are supposed to survive the severe situations with faulty power unit(s) to guarantee the overall healthy operation.

When faults occur in power unit(s) of a CMI, one typical solution is to bypass the failed unit(s) immediately to prevent further damage to the whole system [3, 14-16]. The faulty unit(s) can be cleared easily and rapidly via their bypass facility which is usually a pair of antiparallel thyristors [19]. Hence, the CMI is regenerative. But this bypassing solution has a lot of disadvantages [14-18], i.e. asymmetry of the output voltages, rapid THD increase, and amplitude drop of the fundamental components. It may also cause system over-current and other serious failures such as AC voltage sag, reactive and harmonic current injection, and voltage unbalance. Conventionally, to obtain balanced output voltage and to avoid the above-mentioned problems, the corresponding power units in other normal phases, which have got the same location with the failed ones, are also bypassed simultaneously [3, 14]. This method is feasible yet less efficient because the bypassed healthy units will be a waste of the system potential [14]. Besides, several other solutions are proposed to achieve balanced line voltages without bypassing any healthy units [15-20]. However, most of them suffer from heavy computation burden and increased distortions of the output voltages. Moreover, most of the existing strategies aiming to improve the system performance are only applicable for the Y-connected three-phase structure. Nevertheless, some power electronic devices employ a Δ-connected structure [7-8], even a single-phase system or a multi-phase system.

This paper presents a generic fault-tolerant control strategy to bypass the faulty unit(s) seamlessly. It is valid and universal for the device composed of Carrier Phase Shifting PWM (CPS-PWM) based CMIs, whether it is a single-phase system, a three-phase system (be it Δ-connected or Y-connected) or a multi-phase system. The main idea of this strategy is to adjust the carrier period and simultaneously regulate the DC capacitor voltage and/or the modulation ratio, through which only the faulty power unit(s) will be bypassed and the normal operation of the system can be recovered fast. Furthermore, this proposed strategy is easy and flexible in implementation and the computational burden can be reduced significantly.

This paper is organized as follows. In Section II, the topology and the modulation scheme of CMI are introduced first. In Section III, the ideal control strategy to mitigate the severe consequence of directly bypassing the faulty unit(s) is

Manuscript received June 18, 2018; revised Oct 10, 2018; accepted Jan 28, 2019. Date of current version Feb 8, 2019. The work was supported by National Natural Science Foundation of China (51707091), Scientific Research Foundation for the High-level Personnel (YKJ201613) and Open Research Fund of Jiangsu Collaborative Innovation Center for Smart Distribution Network (XTCX201711), Nanjing Institute of Technology.

Liansong Xiong is with the School of Automation and Jiangsu Collaborative Innovation Center for Smart Distribution Network, Nanjing Institute of Technology, Nanjing 211167, China (e-mail: xiongliansong@163.com).

Liansong Xiong, Fang Zhuo, Xiaokang Liu and Yixin Zhu are with the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: zffz@mail.xjtu.edu.cn).

Xiaokang Liu is with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milan 20133, Italy (e-mail: xiaokang.liu@polimi.it).

Liansong Xiong and Zhao Xu are with the Department of Electrical Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong 999077, China (e-mail: zhao.xu@polyu.edu.hk).

Yixin Zhu is with the School of Internet of Things Engineering, Jiangnan University, Wuxi 214122, China (e-mail: zhuyixin1987@163.com).

described. In Section IV, the CMI output voltage is analyzed quantitatively and in Section V, the generic fault-tolerant control is presented. Its detailed implementation is analyzed and its advantages/disadvantages are presented. In Section VI, the experimental results are provided to demonstrate the effectiveness and superiority of the proposed scheme. Finally, the conclusions of this study are presented in Section VII.

II. Topology and Modulation Scheme of CMI

A CMI consists of N cascaded power units and each individual unit is usually a complete single-phase inverter such as H-bridge (see Fig. 1), Half-bridge and T-type inverters. This paper takes the frequently-used H-bridge inverter as the power unit, and such CMI is also commonly called as a Cascaded H-Bridge (CHB) converter (see Fig. 2) [1, 2].

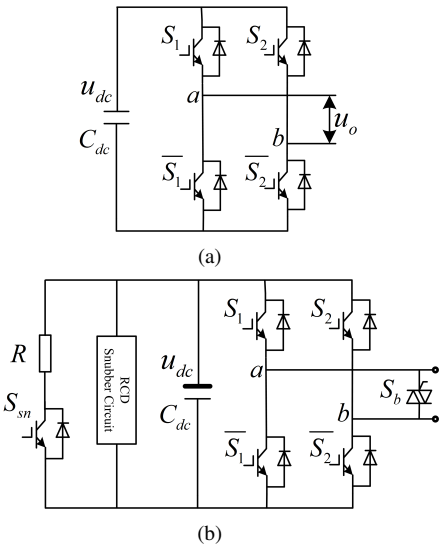


Fig. 1. Topology of a power unit. (a) Circuit of an ideal power unit; (b) Power unit with bypass equipment

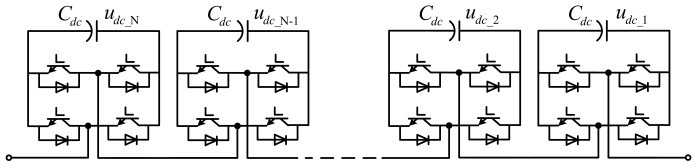


Fig. 2. Topology of a single-phase CMI system

In Fig. 1 (a), u_{dc} is the capacitor voltage and u_o is the output voltage of the power unit; S_1 and $\overline{S_1}$ (S_2 and $\overline{S_2}$) represent the logic signals of the switches in one leg, respectively. Let "1" represent switch on and "0" for off. Therefore, S_τ+$\overline{S_\tau}$=1 ($\tau = 1, 2$). Define that

$$T = S_1 - S_2 \tag{1}$$

Then the relationship between the output voltage u_o and the capacitor voltage u_{dc} is

$$u_o = (S_1 - S_2) \cdot u_{dc} = T \cdot u_{dc} \tag{2}$$

With N cascaded power units, the CMI output voltage u_{CMI} yields

$$u_{\text{CMI}} = \sum_{i=1}^{N} u_{oi} = u_{dc} \sum_{i=1}^{N} T_i \tag{3}$$

where u_{oi} and T_i are the output voltage and the switch logic difference of the i^{th} power unit, respectively.

It can be clearly seen from (3) that the CMI can be regarded as a controlled voltage source and the control variable is T_i. To reduce the harmonics, this paper adopts the CPS-PWM method to modulate the CMI. The CPS-PWM scheme has always been a promising solution for its flexibility in implementation, and CMI can obtain high equivalent switching frequency [1].

The CPS-PWM can be implemented as follows [9]: N power units share a public modulation signal whose amplitude is M and frequency is f_m; the triangle carriers of two adjacent units have a π/N angle deviation; the carriers of two legs in one unit are complementary. Therefore, the equivalent switching frequency increases to $2Nkf_m$ and the CMI output voltage has $(2N + 1)$ levels, where T_c is the carrier period and k is the frequency modulation ratio calculated by

$$k = \frac{1}{f_m \times T_c} \tag{4}$$

III. CMI Fault and Conventional Solutions

Power unit(s) breakdown can be caused by the power unit failure or the grid fault [14]. The former mainly includes open- or short-circuit fault of bridge legs, over-voltage fault, pulse loss, power supply faults, thermal protection, etc [2-3, 5, 11-18]. The latter includes voltage asymmetry, power oscillation, grid overvoltage and so on. Under these conditions, the CMI system cannot operate normally anymore. To ensure the safe operation of the system, the faulty units are usually cut off directly [14, 18].

Merely bypassing the faulty unit(s) will remarkably degrade the system performance [18-20] such as output voltage asymmetry, rapid THD increase, fundamental voltage decrease etc. To avoid this problem and heal the system, a common method in industry is to bypass the same number of units in each normal phase. This method is simple and effective to avoid voltage unbalance. However, it sacrifices the system capacity and cannot maximize the CMI's potential. To improve this situation, the Neutral Shift method is proposed [18-20]. It is applicable for Y-connected structures and can acquire maximum symmetrical line voltages after bypassing the faulty unit(s).

To improve the system reliability, the fault-tolerant ability is usually considered in system design with $n+1$ redundancy. Taking the 10 kV STATCOM as an example, the CMI in the Δ-connected device needs 10 power units and in the Y-connected device needs 7. Both of them have 1 redundant unit. Assume that 2 units in Phase A go wrong and are bypassed immediately. Since the two STATCOMs are both designed with 1 redundant unit, for the $\triangle$-connected device, rated operation needs 9 units and can output 88.8% rated line voltage when 2 failed units are bypassed, accordingly this device cannot operate normally anymore. For the Y-connected device,

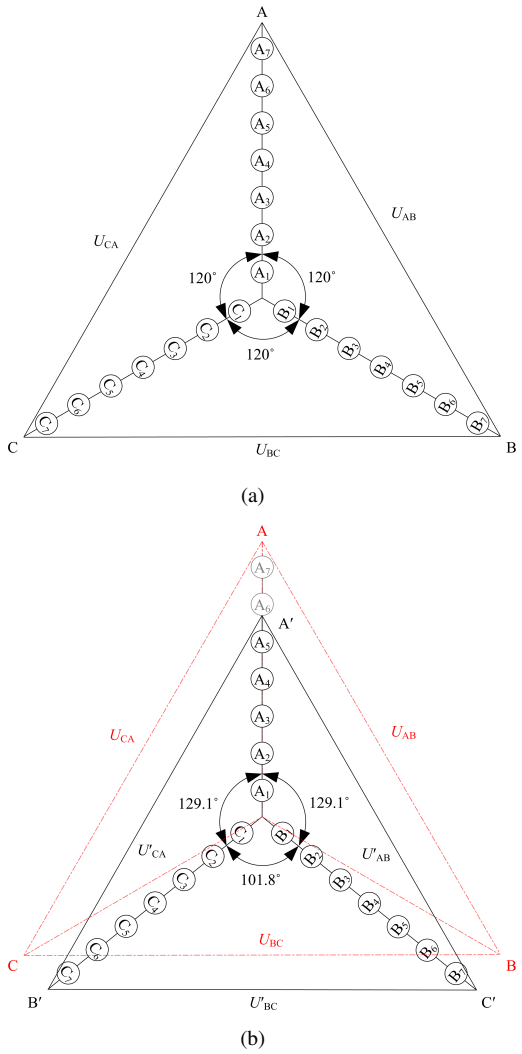


Fig. 3. The adjustment method with 2 failed units. (a) Normal operation; (b) After adjustment.

nevertheless, its phase voltage could be changed flexibly and one of the numerous possible phase voltage groups can make the output line voltage balanced and its peak voltage can exceed the rated line voltage. The available phase voltage group can be sorted by the aforementioned Neutral Shift strategy [18]. The adjusted Y-connected device can output 104.6% rated line voltage by adjusting the phase angle between Phase B and Phase C from 120° to 101.8° (see Fig. 3) and, thus, this device can continue operating normally.

However, this strategy still has some disadvantages. Though the same amplitude of line voltages can be maintained, voltage harmonics increase sharply. It suffers from heavy computation and cannot bring the line voltages back to the rated value precisely. There is always some voltage amplitude drop, which narrows down the operation range of the CMI system. To solve these problems, scholars have presented many advanced solutions based on the Neutral Shift approach, such as adjusting the phase-shift angle of carriers, integrating other modulation methods and control strategies into it and so on [23-27]. These methods can partially address the above mentioned problems and are only applicable for Y-connected structures.

To ensure the normal operation and guarantee high quality power (voltages, currents, power factor, THD and so on) after bypassing the faulty units, a more efficient control strategy should be proposed. It should be applicable for all the CMI system and satisfy the following three conditions:

*1) **Constant equivalent switching frequency**:* The harmonics of the CMI output voltage and current mainly depends on the equivalent switching frequency. After bypassing the fault unit(s), the harmonics of the output voltage/current should be unchanged, therefore, efforts to redesign the passive filters can be saved.

*2) **Constant sampling frequency**:* All the analog-digital chips operate at predefined sampling frequencies to execute the program and to generate the PWM signals. With the fault detection and isolation algorithm, the faulty phase will be rebuilt. But for simplicity, its sampling frequency and controller frequency should be the same with that of the normal phases, benefiting the system control and avoiding unnecessary hardware costs.

*3) **Constant fundamental voltage**:* System with regenerative CMIs mainly works in the current control mode and the current is controlled by CMI output voltages. To generate balanced and rated output currents, the CMI voltage should be maintained.

This paper proposes a generic fault-tolerant strategy, which can bypass the faulty units seamlessly for all the CPS-PWM based CMI systems. The detailed analysis and implementation are provided in the next section.

IV. Modeling of CMI Output Voltage

To obtain the proposed fault-tolerant strategy, the quantitative analysis of the CMI output voltage is carried out first. The modeling of CMI output voltage is based on two basic assumptions. The first one is that each power unit is identical, except for the carrier with a phase difference; the second is that the DC voltage of each unit is constant.

As shown in (3), the CMI voltage is the superposition of the output voltage of each power unit. Therefore, the voltage expression of each unit is obtained first and the CMI output voltage can be deduced accordingly. As shown in Fig. 1 (a), two bridge legs are independent half-bridge inverters and, therefore, the output voltages $u_a(t)$ and $u_b(t)$ can be solved separately. To obtain the expression of $u_a(t)$, the coordinate system of modulating signal and the carrier is selected according to Fig. 4.

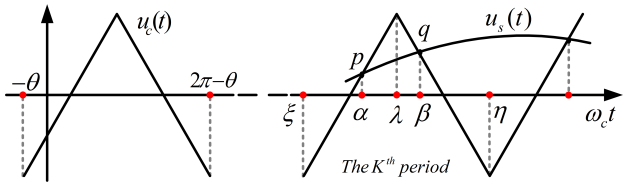


Fig. 4. Carrier and modulating signal in coordinate system

Assume that the expressions of modulation wave $u_s(t)$ and carrier wave $u_c(t)$ are:

$$u_s(t) = M\sin(\omega_s t) \tag{5}$$

$$u_c(t)=\begin{cases}(\omega_c t-\xi)\dfrac{2}{\pi}-1, \xi\le\omega_c t\le\lambda\\ -(\omega_c t-\eta)\dfrac{2}{\pi}-1, \lambda\le\omega_c t\le\eta\end{cases} \tag{6}$$

where ξ, λ, η are the start, middle and end points of the $K^{th}(K=0,1,2,...)$ period, respectively. α and β are the x-coordinates of the intersection points p and q of $u_s(t)$ and $u_c(t)$ in the K^{th} period. They are given by

$$\begin{cases}\xi=2\pi K-\theta\\ \eta=2\pi K-\theta+2\pi\\ \alpha=2\pi K-\theta+\dfrac{\pi}{2}(1+M\sin(\omega_s t))\\ \beta=2\pi(K+1)-\theta-\dfrac{\pi}{2}(1+M\sin(\omega_s t))\\ \lambda=2\pi K-\theta+\pi\end{cases} \tag{7}$$

In terms of the comparison results between $u_s(t)$ and $u_c(t)$ in Fig. 4, $u_a(t)$ can be deduced as

$$u_a(t)=\begin{cases}\frac{u_{dc}}{2} & \xi\le\omega_c t\le\alpha,\beta\le\omega_c t\le\eta\\ -\frac{u_{dc}}{2} & \alpha\le\omega_c t\le\beta\end{cases} \tag{8}$$

Based on Dual Fourier Series Theory and Bessel Theory, the expression of $u_a(t)$ is given by

$$\begin{aligned}u_a(t)=&M\frac{u_{dc}}{2}\sin(\omega_s t)+\frac{2u_{dc}}{\pi}\sum_{m=1,3,5,...}^{\infty}A(m)+\\ &\frac{2u_{dc}}{\pi}\sum_{m=1,2,3,...}^{\infty}\sum_{n=\pm1,\pm2,\pm3,...}^{\pm\infty}B(m,n)\sin\frac{(m+n)\pi}{2}\end{aligned} \tag{9}$$

where

$$A(m)=\frac{J_0(\frac{m\pi M}{2})}{m}\sin\frac{m\pi}{2}e^{-jm\theta}\cos(mk\omega_s t),$$

$$B(m,n)=\frac{J_n(\frac{m\pi M}{2})}{m}e^{-jm\theta}\cos[(mk+n)\omega_s t-\frac{n\pi}{2}]$$

Similarly, the time-domain expression of $u_b(t)$ can be deduced and the initial phase of carrier wave turns to θ+180°.

$$\begin{aligned}u_b(t)=&-M\frac{u_{dc}}{2}\sin(\omega_s t)+\frac{2u_{dc}}{\pi}\sum_{m=1,3,5,...}^{\infty}A(m)+\\ &\frac{2u_{dc}}{\pi}\sum_{m=1,2,3,...}^{\infty}\sum_{n=\pm1,\pm2,\pm3,...}^{\pm\infty}\sin\frac{(m-n)\pi}{2}B(m,n)\end{aligned} \tag{10}$$

Then the output voltage u_{oi} of the i^{th} unit is:

$$\begin{aligned}u_{oi}(t)=&u_a(t)-u_b(t)=Mu_{dc}\sin(\omega_s t)+\\ &\frac{4u_{dc}}{\pi}\sum_{m=1,2,3,...}^{\infty}\sum_{n=\pm1,\pm2,\pm3,...}^{\pm\infty}\cos\frac{m\pi}{2}\sin\frac{n\pi}{2}B(m,n)\end{aligned} \tag{11}$$

It holds that

$$\begin{aligned}&\cos[(mk+n)\omega_s t-\frac{n\pi}{2}]\\ =&\cos[(mk+n)\omega_s t]\cos\frac{n\pi}{2}+\sin[(mk+n)\omega_s t]\sin\frac{n\pi}{2}\end{aligned} \tag{12}$$

Moreover, when n is odd,

$$\cos\frac{n\pi}{2}=0 \tag{13}$$

Based on (12) and (13), (11) can be simplified as

$$\begin{aligned}u_{oi}(t)=&Mu_{dc}\sin(\omega_s t)+\\ &\frac{4u_{dc}}{\pi}\sum_{m=1,2,3,...}^{\infty}\sum_{n=\pm1,\pm2,\pm3,...}^{\pm\infty}(\sin\frac{n\pi}{2})^2e^{-jm\theta}C(m,n)\end{aligned} \tag{14}$$

where

$$C(m,n)=\frac{J_n(\frac{m\pi M}{2})}{m}\cos\frac{m\pi}{2}\sin[(mk+n)\omega_s t]$$

Obviously, when m and n are odd,

$$\begin{cases}\cos\dfrac{m\pi}{2}=0\\ (\sin\dfrac{n\pi}{2})^2=1\end{cases} \tag{15}$$

When m and n are both even numbers,

$$\begin{cases}\cos\dfrac{m\pi}{2}=(-1)^{m/2}\\ (\sin\dfrac{n\pi}{2})^2=0\end{cases} \tag{16}$$

Consequently, (11) can be further simplified as

$$\begin{aligned}u_{oi}(t)=&Mu_{dc}\sin(\omega_s t)+\\ &\frac{4u_{dc}}{\pi}\sum_{m=2,4,6,...}^{\infty}\sum_{n=\pm1,\pm3,\pm5,...}^{\pm\infty}C(m,n)e^{-jm\theta}\end{aligned} \tag{17}$$

N power units with the same DC voltage are cascaded and modulated by the CPS-PWM method. The initial phases of carriers have a $\frac{\pi}{N}$ difference with each other, namely, the initial phases are θ, $(\theta+\frac{\pi}{N})$, $(\theta+\frac{2\pi}{N})$, $(\theta+\frac{3\pi}{N})$, ..., $(\theta+\frac{(N-1)\pi}{N})$ sequentially. For convenience, assume θ equals to zero. Then substitute the initial phase into (17), and $u_{\text{CMI}}(t)$ is obtained:

$$\begin{aligned}u_{\text{CMI}}(t)=&\sum_{i=1}^{N}u_{oi}(t)=NMu_{dc}\sin(\omega_s t)+\\ &\frac{4u_{dc}}{\pi}\sum_{m=2,4,6,...}^{\infty}\sum_{n=\pm1,\pm3,\pm5,...}^{\pm\infty}\sum_{i=1}^{N}e^{-j\frac{m(i-1)\pi}{N}}C(m,n)\end{aligned} \tag{18}$$

It holds that

$$\sum_{i=1}^{N}e^{-j\frac{m(i-1)\pi}{N}}=\begin{cases}N & m=2KN\\ 0 & m\ne2KN\end{cases}(K=1,2,3,\cdots) \tag{19}$$

Therefore, (18) could be simplified as

$$\begin{aligned}u_{\text{CMI}}(t)=&\sum_{i=1}^{N}u_{oi}=NMu_{dc}\sin(\omega_s t)+\\ &\frac{4Nu_{dc}}{\pi}\sum_{m=2N,4N,6N,...}^{\infty}\sum_{n=\pm1,\pm3,\pm5,...}^{\pm\infty}C(m,n)\end{aligned} \tag{20}$$

u_{CMI} can be divided into the required fundamental component and the harmonic component. The latter is needless and must be filtered out. The harmonic component indicates that the CMI modulated by CPS-PWM can eliminate the low-order harmonics of number below $(2kN\pm1)$. The main harmonics are high-order ones, yet their contents are very low. Hence, the CMI voltage satisfies the requirement of low THD.

V. Proposed Generic Fault-tolerant Control for CPS-PWM Based CMI System

A. Analysis on Generic Fault-tolerant Control Strategy

Before analyzing the generic fault-tolerant control strategy, the PWM generation method for CMI should be demonstrated first. By assuming that CMI is composed of 5 power units, the PWM generation process is illustrated in Fig. 5.

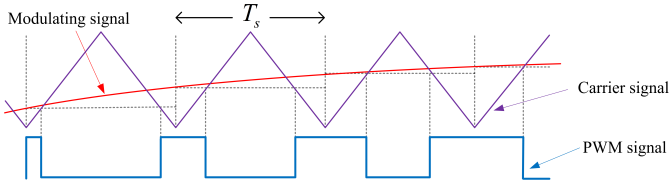


Fig. 5. PWM generation method

Let the sampling period be T_s; the carrier period before and after adjustment be T_c and $T_c^{'}$, respectively. Then, the sampling interval between two adjacent units is T_s, and the sampling interval of each unit is $5T_s$. Take the left leg of the 1^{st} unit as an example and its PWM generation process is illustrated in Fig. 6.

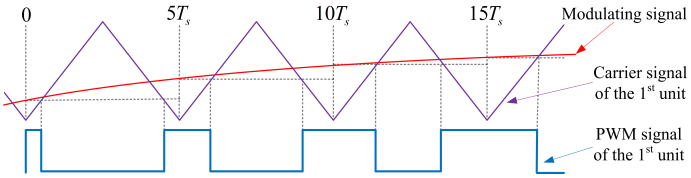


Fig. 6. PWM generation method of left leg in 1^{st} unit

If we use the time axis to demonstrate the sampling time sequence, the pulse generation time sequence of these 5 units is shown in Fig. 7. The purple points represent the pulse generation time of the 1^{st} unit.

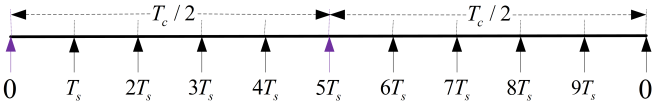


Fig. 7. Pulse time sequence under normal condition

After bypassing the faulty unit and before implementing auxiliary control algorithm, the pulse generation time sequence is illustrated in Fig. 8. In such case, the 5^{th} unit of CMI has been cleared.

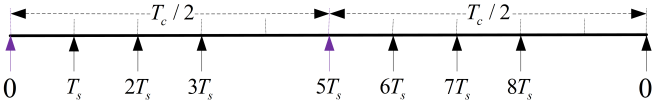


Fig. 8. Pulse time sequence after bypassing faulty unit and before implementing additional control strategy

As illustrated in Fig. 8, the sampling interval between two adjacent units, which may be T_s or $2T_s$, is no longer fixed. To ensure the immutability of the sampling frequency and the sampling interval between two adjacent units T_s, the pulse generation time sequence after implementing additional control algorithm is indicated in Fig. 9.

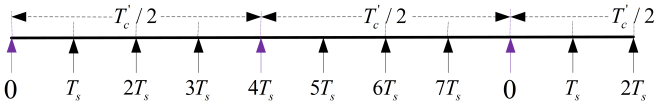


Fig. 9. Pulse time sequence after additional control strategy implementing

Obviously, the carrier frequency increases after implementing the additional control algorithm. It holds that

$$T_c^{'} = \frac{4}{5}T_c \tag{21}$$

Generally, assume the CMI with n power units is modulated by the CPS-PWM method and its carrier period is T_c. Accordingly, when $m(n > m)$ faulty units are bypassed, the carrier period after adjustment should be

$$T_c^{'} = \frac{n-m}{n}T_c \tag{22}$$

Quite evidently, when the fault-tolerant strategy satisfies the conditions above, the equivalent switching frequency and the sampling frequency can keep constant, and the harmonics of CMI voltage are virtually unaffected. The proof is as follows.

Based on the CPS-PWM theory, the sampling interval T_s of CMI is given by:

$$T_s = \frac{T_c}{2n} \tag{23}$$

Accordingly, the pre-fault sampling interval between two adjacent units is also T_s, which is also given by (23). When the faulty units are cleared later, the carrier period must be adjusted immediately according to (22). After the fault-tolerant strategy implementation, the new sampling interval $T_s^{'}$ is calculated by:

$$T_s^{'} = \frac{T_c^{'}}{2(n-m)} = \frac{T_c}{2n} = T_s \tag{24}$$

In this sense, the sampling interval is immutable and the generic fault-tolerant strategy can achieve constant sampling frequency. Therefore, there is no need to change the controller frequency and the sampling frequency, and only the carrier period automatically changes.

Let the frequency of modulating signal be f_m and take the inverter leg as the fundamental element. Thus, the frequency modulation ratio before adjustment k is given by (4). The ratio after adjustment $k^{'}$ can be deduced by

$$k^{'} = \frac{1}{f_m T_c^{'}} = \frac{1}{f_m \frac{n-m}{n} T_c} = \frac{n}{(n-m) f_m T_c} = \frac{nk}{n-m} \tag{25}$$

According to the CPS-PWM theory, the equivalent switching frequency before adjustment f_s is calculated by

$$f_s = 2nkf_m \tag{26}$$

Based on (25) and (26), the equivalent switching frequency after the fault-tolerant control implementation $f_s^{'}$ is

$$f_s^{'} = 2(n-m)k^{'} f_m = 2nkf_m = f_s \tag{27}$$

Hence, the generic fault-tolerant strategy can achieve constant equivalent switching frequency.

Based on the rigorous theoretical analysis in Section IV, cascading n power units can eliminate the low harmonics below $(2nk \pm 1)$. With this conclusion and (25), the following equation can be deduced as

$$2(n-m)k^{'} \pm 1 = 2(n-m)\frac{nk}{n-m} \pm 1 = 2nk \pm 1 \quad (28)$$

Accordingly, after the adjustment based on the generic fault-tolerant strategy, the device can also eliminate the harmonics with orders below $(2nk \pm 1)$. The spectral characteristics of the CMI output voltage are virtually unchanged. Accordingly, after being filtered by the linking inductor of CMI, the THD of CMI output current will also keep unaltered or increase slightly, satisfying the requirement of constant harmonic characteristics.

Simulation results are provided for a better explanation, where the built CMI has 10 power units and the carrier frequency is 1 kHz. Assume that at 0.06 s, a fault occurs on the 10^{th} unit and, after that, this unit is bypassed directly. The carrier period before and after adjustment are 1 ms and 0.9 ms, respectively, as illustrated in Fig. 10. The simulation result is in accordance with (22). The simulation shows the sampling frequency and the equivalent switching frequency of CMI keep 20 kHz all the time, ensuring the principles of constant sampling frequency and constant equivalent switching frequency.

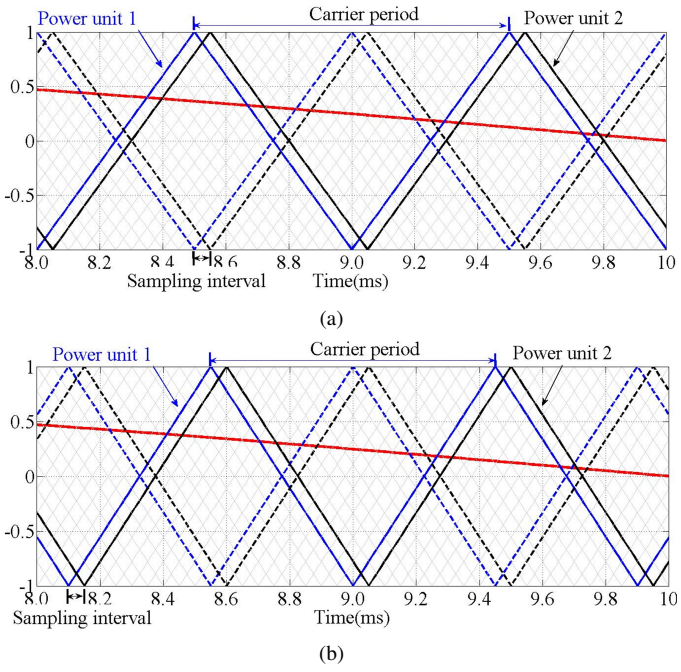


Fig. 10. Modulating signal and phase shifted carriers. (a) before adjustment; (b) after adjustment.

To realize the generic fault-tolerant control strategy, the 3^{rd} principle must also be satisfied. Assume that the DC voltage of each unit is U_{dc} and the modulation ratio is M. From (20), the amplitude U_f of the fundamental component of the CMI output voltage u_{CMI} can be calculated as

$$U_f = nMU_{dc} \quad (29)$$

Therefore, the main aspects that affect the CMI fundamental voltage amplitude are the number of power units n, the modulation ratio M and the DC voltage of each unit U_{dc}. It is feasible to realize the constant CMI fundamental voltage amplitude, before and after bypassing the faulty units, by controlling M and/or U_{dc}.

After bypassing m faulty units, the new amplitude of the fundamental component of the CMI voltage $U_f^{'}$ is given by

$$U_f^{'} = (n-m)MU_{dc} \quad (30)$$

Let

$$U_f^{'} = U_f \quad (31)$$

Case 1: changing the DC voltage U_{dc} only

Assume the DC voltage after change is $U_{dc}^{'}$, then

$$U_f^{'} = (n-m)MU_{dc}^{'} \quad (32)$$

By substituting (29), (32) into (31), the new DC voltage $U_{dc}^{'}$ after adjustment can be obtained as

$$U_{dc}^{'} = k_U U_{dc} = \frac{n}{n-m}U_{dc} \quad (33)$$

Case 2: changing the modulation ratio M only

Assume the modulation ratio after change is $M^{'}$. Then

$$U_f^{'} = (n-m)M^{'}U_{dc} \quad (34)$$

By substituting (29), (34) into (31), the new modulation ratio $M^{'}$ after adjustment can be obtained as

$$M^{'} = k_M M = \frac{n}{n-m}M \quad (35)$$

Case 3: changing the DC voltage U_{dc} and the modulation ratio M simultaneously

Assume the DC voltage and the modulation ratio after change are $U_{dc}^{'}$ and $M^{'}$, respectively, then

$$U_f^{'} = (n-m)M^{'}U_{dc}^{'} \quad (36)$$

By substituting (29), (36) into (31), it can be deduced that the new DC voltage $U_{dc}^{'}$ and the new modulation ratio $M^{'}$ after adjustment must satisfy the following equation

$$M^{'}U_{dc}^{'} = k_M k_U MU_{dc} = \frac{n}{n-m}MU_{dc} \quad (37)$$

Based on the analysis above, the generic fault-tolerant strategy can be obtained as follows: 1) adjust the carrier frequency first to satisfy the 1^{st} and 2^{nd} principles and 2) adjust the modulation ratio and/or the DC voltage to satisfy the 3^{rd} principle.

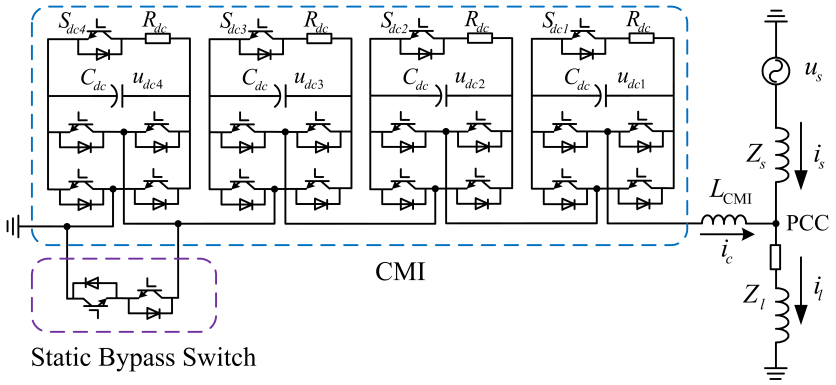


Fig. 11. System configuration of single-phase cascaded STATCOM.

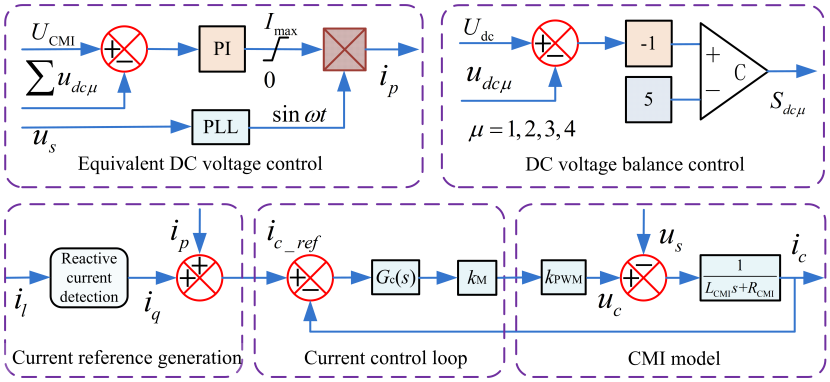


Fig. 12. System control strategy of single-phase cascaded STATCOM.

B. Comparative Analysis of CMI Voltage Control Methods

In general, adjusting the modulation ratio is the simplest and fastest way, since it can be implemented by simply modifying the modulation ratio in the controller software. On the contrary, concerning the other methodologies, charging or discharging the DC capacitor of each power unit is the only way to realize the DC voltage change. Consequently, the response time is long and it is not beneficial to realize fast fault recovery. The detailed comparative analysis is provided as follows.

Method I : changing the DC voltage only

1) Benefits: The only advantage it has is the simplicity.

2) Defects: (1) It is only applicable in the devices whose DC voltage is adjustable. (2) When the difference between n and m is small, k_U is large and the adjusted DC voltage may exceed the designed maximum value in this situation. (3) Charging or discharging the DC capacitors leads to the long response time, which is not beneficial to fast fault riding through.

Method II : changing the modulation ratio only

1) Benefits: This method is the simplest and it can be immediately realized by adjusting the modulation ratio M in the software. Accordingly, the response of the fault-tolerant control is the fastest.

2) Defects: The variation range of the modulation ratio M is narrow, causing inability in some special cases. The modulation ratio after adjustment $M^{'}$ is generally smaller than 1 (except the SVPWM), i.e.

$$M^{'} = \frac{n}{n-m} M < 1 \tag{38}$$

In this sense, the range of the modulation ratio before adjustment M is:

$$M < \frac{n-m}{n} \leq 1 \tag{39}$$

Besides, to increase the DC voltage utilization factor, the modulation ratio M in practice is usually larger than 0.8, i.e.

$$0.8 < M < \frac{n-m}{n} \quad \Rightarrow \quad n > 5m \tag{40}$$

It is apparent from (40) that the CMI which only adopts Method II should contain $5m$ power units at least if m redundant units are considered. In this sense, this method is inappropriate when the CMI power units are less than 5.

Method III : changing the DC voltage and modulation ratio simultaneously

Generally, system design must consider enough capacity margin of the DC voltage and modulation ratio to cope with the worst operation situation. Therefore, Method III can utilize the utmost of the capacity margin and overcome the limitation of Method I and Method II, especially when the faulty unit number m is large. Considering it is easier to adjust the modulation ratio, the suggestion is raising the modulation ratio first and then adjusting the DC voltage U_{dc} when M approaches 1. The defect is that this method is a little complicated because two variables are adjusted simultaneously.

VI. Experimental Verification

Due to the limitation of experimental conditions, the proposed fault-tolerant strategy was verified on a single-phase STATCOM (see Fig. 11). The main parameters are listed in Table I. The parallel DC-side resistor $R_{\rm dc}$ is utilized to control the DC capacitor voltage $u_{dc\mu}$ $(\mu = 1, 2, 3, 4)$. Besides, the bidirectional switch is adopted to bypass the faulty unit.

TABLE I
Parameters of Experimental STATCOM

Grid voltage	220 V / 50 Hz	Carrier frequency f_c	10 kHz
Inductive load Z	10 Ω / 60 mH	Power unit number N	4
Linking inductor	0.01 Ω / 60 mH	DC-side resistor $R_{\rm dc}$	10 Ω
DC capacitor	3300 μF	DC capacitor voltage	240 V

The system control strategy is shown in Fig. 12, where $U_{\rm dc}$ is the rated DC voltage of each unit. The reference signal of the current control loop is generated combining the detected reactive current and the active current signal generated through equivalent DC voltage control [28]. The equivalent DC voltage of CMI $U_{\rm CMI}$ is the sum of all the DC voltages of each unit. Besides, the DC capacitor voltage balance is achieved by controlling the parallel IGBT on the DC side.

To guarantee the safety of experimental instruments, large margin of DC voltage is reserved. Besides, the CMI is well designed to withstand large enough current such that the current loop regulator is not saturated all the time and, thus, the CMI voltage can be controlled linearly. It should be emphasized that large margin is not the general case in real applications.

Experiments are performed concerning the three fault-tolerant strategies presented above. The DC capacitor voltage is 240V under normal conditions. A fault occurs on one power unit, which is bypassed after then. The control signal is unchanged in the red rectangular region, and the output voltage is distorted (see Fig. 13, cyan curve), leading to disturbances in output current (see Fig. 13, purple curve), as expected. If the carrier frequency is adjusted, the wave quality of CMI voltage/current can quickly return to its normal operation, as shown outside the red rectangular region.

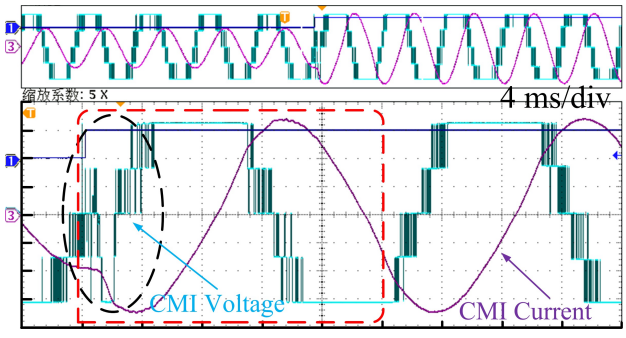


Fig. 13. CMI voltage/current with/without fault-tolerant control strategy.

A. Adjusting DC Voltage Only

To change the DC capacitor voltage, charging and discharging processes are present. The charging current should be kept constant to the maximum design current of CMI to improve the dynamic speed. Accordingly, the equivalent DC voltage controller undergoes three stages during the entire experiment process (see Fig. 14, blue curve): 1) linear region I; 2) nonlinear region in which the charging current is kept constant and 3) linear region II.

In Fig. 14, a fault occurs at t_1 and the CMI current increases accordingly. The faulty unit is detected and then bypassed. After that, Method I is harnessed to recover the normal operation. Since the faulty unit is bypassed, the sum of all the DC capacitor voltages (also the equivalent DC voltage of CMI, $U_{\rm CMI}$) is considerably smaller than its reference value (960V), and the PI regulator of equivalent DC voltage loop readjusts its output immediately (see Fig. 14, t_1-t_2 blue curve). Since the input error is large, the outer voltage loop controller saturates soon (see Fig. 14, t_2-t_4 blue curve), leading to the maximum current output (see Fig. 15(a)). Meanwhile, huge power is injected to CMI from the grid (see Fig. 15(b)). In this case, the power is totally absorbed by $R_{\rm dc}$ under DC voltage balance control if the DC voltage $U_{\rm dc}$ is not adjusted, such that $U_{\rm dc}$ is kept its reference value (240 V). Consequently, it's impossible for $U_{\rm CMI}$ to reach its reference value (960 V). The voltage regulator is kept saturated and CMI cannot return to its normal operation.

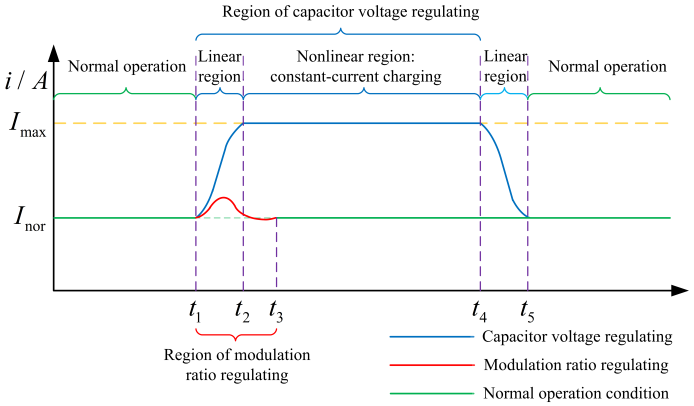


Fig. 14. CMI currents with different fault-tolerant control strategies.

On the contrary, by adjusting the DC voltage $U_{\rm dc}$, CMI can return to its normal operation in a short time. According to (38), $U_{\rm dc}$ should be set as 320 V instead of 240 V. In such case, the injected power charges the capacitors with constant current, leading to linear increase of DC voltage (see Fig. 15(c)). When $U_{\rm dc}$ approaches to 320 V (also $U_{\rm CMI}$ approaches to its reference value, i.e. 960V), the equivalent DC voltage regulator becomes unsaturated and operates in the linear region (see Fig. 14, t_4-t_5 blue curve). Finally, $U_{\rm dc}$ reaches 320 V (and $U_{\rm CMI}$ 960 V), and CMI returns to normal.

It is noted that the saturation time of regulator is mainly dependent on the charging time of capacitors. In this experiment, $U_{\rm dc}$ increases (from 240 V to 320 V) with notable voltage change rate (33%) and, thus, the capacitor charging time is long. Therefore, Method I is suitable for the cases with slight changes of DC voltage.

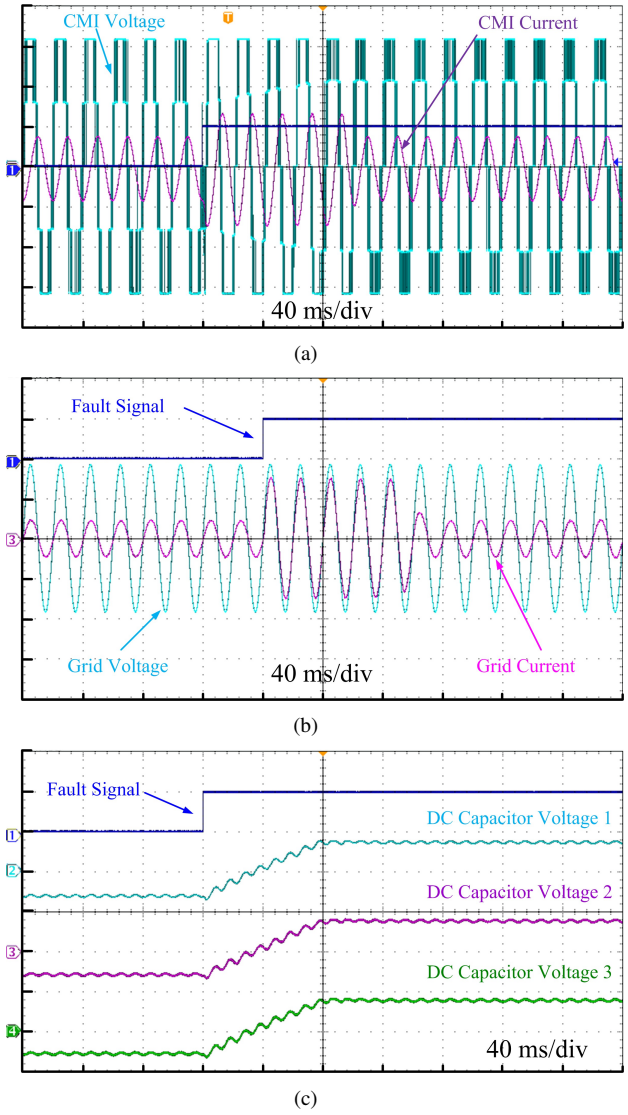


Fig. 15. Experimental results of Method I. (a) CMI output voltage/current; (b) Grid voltage/current; (c) DC Capacitor Voltages.

B. Adjusting Modulation Ratio Only

When only the modulation ratio is changed, no capacitor charging/discharging is required and the response speed is significantly improved, and the CMI current is effectively regulated. In this experiment, the voltage regulator is working in the linear region (i.e., unsaturated) all the time (see Fig. 14, t_1-t_3 red curve). After bypassing the faulty unit, Method II is enabled to bring CMI to its normal operation. U_{CMI} should be revised to 720 V (240V$\times$3) according to (41), and k_{M} should be 4/3 (see Fig. 16(a)). The input error is small in this case, hence the equivalent DC voltage controller works in the linear region. Consequently, the CMI current is effectively controlled all the time (see Fig. 16(b)), and the grid current is virtually unaffected (see Fig. 16(c)). U_{dc} keeps its reference value (240 V) under DC voltage balance control, as shown in Fig. 16(d). It is evident that the influence of faulty unit clearance on system operation is minor with Method II, and CMI returns to its normal state in virtually no time.

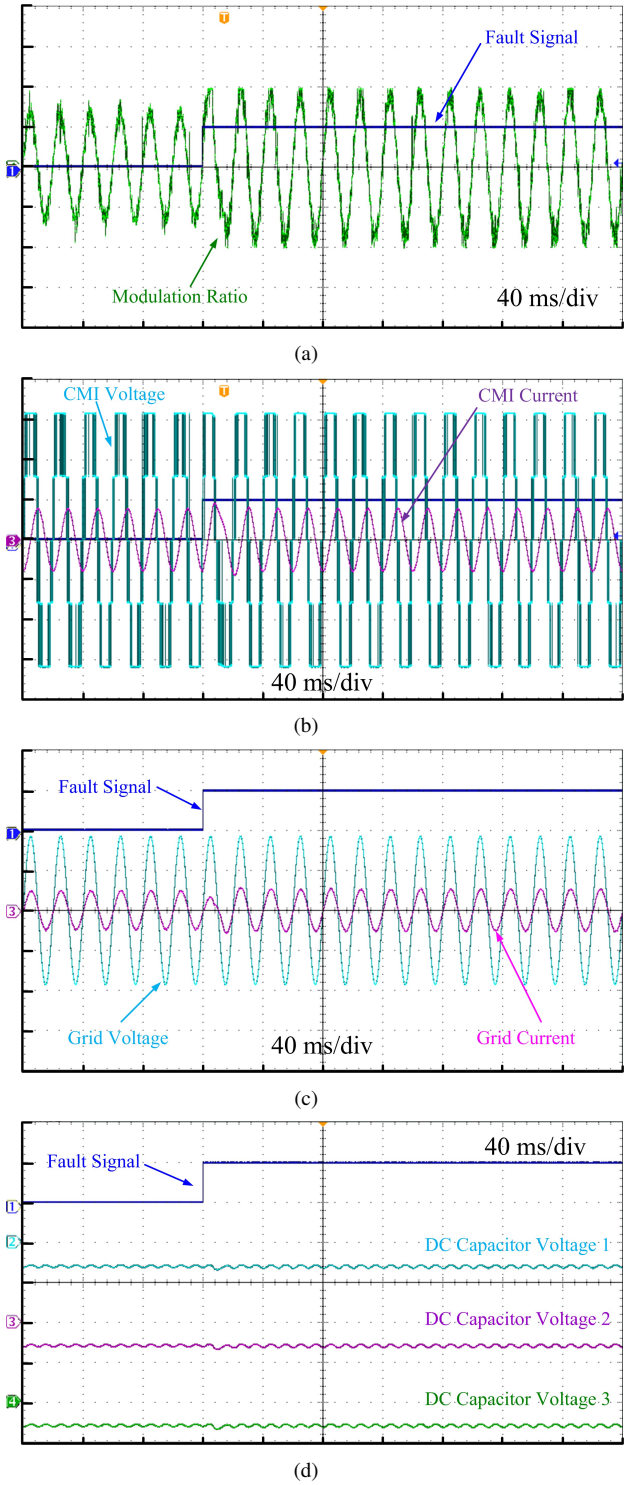


Fig. 16. Results of Method II. (a) Modulation ratio; (b) CMI voltage/current; (c) Grid voltage/current; (d) DC Voltages.

C. Adjusting DC Voltage and Modulation Ratio Together

In this case, U_{dc} is increased from 240 V to 280 V, and k_{M} is adjusted to 8/7 according to (37). The CMI current response is in between Experiment A and B, and the CMI current is similar to that of Experiment A, i.e. 3 stages are also experienced. In comparison to experiment A, the U_{dc} change (16.7% in this case) is smaller and, thus, CMI returns to

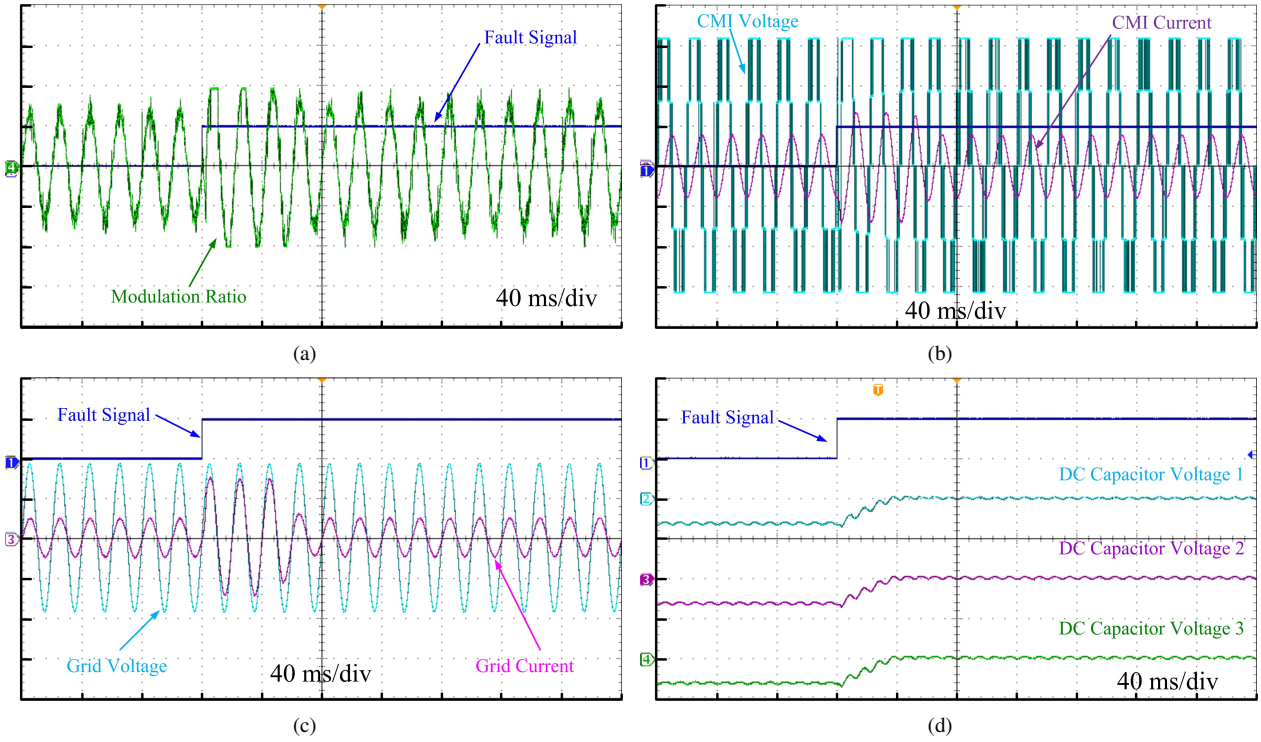


Fig. 17. Results of Method III. (a) Modulation ratio; (b) CMI voltage/current; (c) Grid voltage/current; (d) DC Voltages.

normal in a shorter time (3 grid cycles). The modulation ratio, CMI current, grid current and DC voltage $U_{\rm dc}$ are illustrated in Fig. 17. It is apparent that Method III is better in utilizing the the abundant device capacity (i.e. the abundant DC voltage as well as modulation ratio) and, thus, CMI is able to recover in a shorter time.

It should be specifically stated that the fault-tolerant control proposed in this paper actually uses the safety margin reserved. Once the power unit of the CMI system is bypassed, it means that the system's safety margin is reduced, and the CMI system's ability to resist fault disturbances will be weakened. Therefore, when the power unit is bypassed, it should look for a suitable time (such as during CMI system outage or routine maintenance) and replace the bypassed power unit as soon as possible to restore the safety margin of the CMI system.

VII. Conclusion

Bypassing faulty power units of the regenerative CMI directly, depending on the modulation strategy employed, may results in a series of adverse influences, which are harmful to the reliability and safety of the CMI system. To bypass the faulty units seamlessly when CPS-PWM is applied, the generic fault-tolerant control strategy is presented. The experimental results verify the effectiveness and the superiority of the proposed strategy. This paper obtains the following key conclusions:

1) To ensure that the device composed of regenerative CMIs can ride through the faulty unit(s) isolation seamlessly, an effective control algorithm, such as the fault-tolerant strategy proposed in this paper, must be implemented immediately.
2) To bypass the faulty units seamlessly, the fault-tolerant control should satisfy at least three principles, i.e. constant equivalent switching frequency, constant sampling frequency and constant fundamental voltage amplitude. To this end, the generic fault-tolerant control strategy must adjust the carrier period and simultaneously change the CMI DC voltage and/or the modulation ratio.
3) The proposed control strategy is valid and universal for the device composed of CPS-PWM based CMIs to ride through the faults seamlessly, whether it is a single-phase system, a three-phase system (be it Δ-connected or Y-connected) or a multi-phase system. It is of utmost importance to increase the stability and reliability of the devices with CMIs.

References

[1] Mariusz M., Gopakumar K., Rodriguez J., and Marcelo A. P., " A survey on cascaded multilevel inverters," *IEEE Trans. on Ind. Electron.*, 2010, 57(7): 2197-2206.

[2] Lamb J. and Mirafzal B., "Open-Circuit IGBT Fault Detection and Location Isolation for Cascaded Multilevel Converters," *IEEE Trans. on Ind. Electron.*, vol. 64, no.6, pp. 4846-4856, Jun. 2017.

[3] Surin K., and Leon M. T., "Fault diagnosis and reconfiguration for multilevel inverter drive using AI-based techniques," *IEEE Trans. on Ind. Electron.*, 2007, 54(6): 2954-2968.

[4] Abolhassani M., "Modular Multipulse Rectifier Transformers in Symmetrical Cascaded H-Bridge Medium Voltage Drives," *IEEE Trans. on Power Electron.*, vol. 27, no. 2, pp. 698-705, Feb. 2012.

[5] Khomfoi S. and Tolbert L. M., "Fault Detection and Reconfiguration Technique for Cascaded H-bridge 11-level Inverter Drives Operating under Faulty Condition," *7th Int. Conf. Power Electron. Drive Syst.*, Bangkok, 2007, pp. 1035-1042.

[6] Burhan G., and Muammer E., "Cascaded multilevel converter-based transmission STATCOM: system design methodology and development of a 12 kV 12 MVAr power stage," *IEEE Trans. on Power Electron.*, 2013, 28(11)4930-4950.

[7] He Z. et al., "Reactive Power Strategy of Cascaded Delta-Connected STATCOM Under Asymmetrical Voltage Conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 784-795, June 2017.

[8] Jung J. J., Lee J. H., Sul S. K., et al, "DC Capacitor Voltage Balancing Control for Delta-Connected Cascaded H-Bridge STATCOM Considering Unbalanced Grid and Load Conditions," *IEEE Trans. on Power Electron*., 2018, 33(6): 4726-4735.

[9] Laxman M., Shigenori I., and Akagi H., "A transformerless energy storage system based on a cascade multilevel PWM converter with star configuration," *IEEE Trans. Ind. Appl.*, 2008 44(5): 1621-1630.

[10] Michail V., and Alfred R., "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Trans. on Power Electron*., 2015, 30(1)163-175.

[11] Song Y. and Wang B., "Survey on Reliability of Power Electronic Systems," *IEEE Trans. on Power Electron*., vol. 28, no. 1, pp. 591-604, Jan. 2013.

[12] Choi U. M., Blaabjerg F. and Lee K. B., "Study and Handling Methods of Power IGBT Module Failures in Power Electronic Converter Systems," *IEEE Trans. on Power Electron*., vol. 30, no. 5, pp. 2517-2533, May 2015.

[13] Anand A., Raj N., George S. and Jagadanand G., "Open switch fault detection in Cascaded H-Bridge Multilevel Inverter using normalised mean voltages," *IEEE 6th Int. Conf. Power Syst. (ICPS)*, New Delhi, 2016, pp. 1-6.

[14] Pablo L., Thierry A. M., Jose R., et al, "Survey on fault operation on multilevel inverters," *IEEE Trans. on Ind. Electron*., 2010, 57(7): 2207-2218.

[15] Surin K., and Leon M. T., "Fault diagnostic system for a multilevel inverter using a neural network," *IEEE Trans. on Power Electron*., 2007, 22(3)1062-1069.

[16] Mtepele K. O., Campos D. U., Fernandez A. V. and Pecina J. A., "Fault tolerant controller for a generalized n-level CHB multilevel converter," *13th Int. Conf. Power Electron. (CIEP)*, Guanajuato, 2016, pp. 75-80.

[17] Atousa Y., Hossein S., Mariesa L. C., and Mehdi F., "Fault detection and mitigation in multilevel converter STATCOMs," *IEEE Trans. on Ind. Electron*., 2011, 58(4): 1307-1315.

[18] Hammond P. W., "Enhancing the reliability of modular medium voltage drives," *IEEE Trans. on Ind. Electron.*, 2002, 49(5): 948-954.

[19] Rodriguez J., Lai J. S., Peng F. Z., "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. on Ind. Electron.*, 2002, 49(4): 724-738.

[20] Jos R., Peter W. Hammond, Jorge P., et al, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. on Ind. Electron*., 2005, 52(4): 1080-1085.

[21] Hossein I. E., Shahrokh F., Schanen J. L., and Mahboubeh K. F., "A fault-tolerant control strategy for cascaded H-bridge multilevel rectifiers," *J. Power Electron.*, 2010, 10(1): 34-42.

[22] Ouni S., "A fast and simple method to detect short circuit fault in cascaded H-bridge multilevel inverter," *IEEE Int. Conf. Ind. Technol. (ICIT)*, Seville, 2015, pp. 866-871.

[23] Manjunath T. G., and Kusagur A., "Performance evaluation of Modified Genetic Algorithm over Genetic Algorithm implementation on fault diagnosis of Cascaded Multilevel Inverter," *Int. Conf. Condition Assessment Techniques in Electr. Syst. (CATCON)*, Bangalore, 2015, pp. 51-56.

[24] Song W. C., and Alex Q. H., "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM," *IEEE Trans. on Ind. Electron.*, 2010, 57(8): 2700-2708.

[25] Surin K., 'A reconfiguration technique for cascaded H-bridge multilevel inverter drives," *IEEE ECTI-CON Conf. Rec*., Krabi, Thailand, 2008

[26] An Q. T., Sun L., and Sun L. Z., "Current residual vector-based open-switch fault diagnosis of inverters in PMSM drive systems," *IEEE Trans. on Power Electron*., 2015, 30(5):2814-2827.

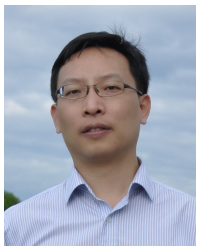
[27] Deng F. J., Chen Z., Mohammad K., and Zhu R. W., "Fault detection and localization method for modular multilevel converters," *IEEE Trans. on Power Electron*., 2015, 30(5):2721-2732.

[28] Xiong L. S. and Zhuo F., "Chopper Controller Based DC Voltage Control Strategy for Cascaded Multilevel STATCOM," *J. Electr. Eng. Technol*., 2014, 9(9):576-588.

Liansong Xiong (S'12-M'16) was born in Sichuan, China, in 1986. He received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from Xi'an Jiaotong University (XJTU), Xi'an, China, in 2009, 2012 and 2016, respectively. In July 2014, He joined the School of E-learning, XJTU, as a Part-Time Faculty. In June 2016, he joined the School of Automation, Nanjing Institute of Technology (NJIT), introduced in High-Level Academic Talent Plan of NJIT. Since November 2017, he is with the Department of Electrical Engineering, The Hong Kong Polytechnic University (PolyU), as a Research Associate in Power System Laboratory. His current research interests are power quality, multi-level converter, renewable energy generation, micro-grid, stability analysis of grid-tied inverter dominated power systems, etc. He is the first author of 8 papers indexed by SCI and more than 20 papers indexed by EI. He has received Excellent Paper Award 6 times in academic conferences and National Scholarship for Graduate Students in three consecutive years. He was honored with the Author of Excellent Doctoral Dissertation of XJTU and Shaanxi Province in 2018, the Excellent Reviewer of High Voltage Engineering (2017-2018), the Outstanding Graduates of XJTU in 2015, and the Excellent Writer of Proceedings of CSEE in 2015. Dr. Xiong is a Senior Member of China Electrotechnical Society and a member of China Power Supply Society.

Fang Zhuo (M'00) was born in in Shanghai, China, on May, 1962. He received his B.S. degree in Automatic Control from Xi'an Jiaotong University (XJTU) in 1984, and then he joined XJTU. In 1989 and 2001, he received the M.S. and Ph.D. degree respectively in Electrical Engineering in XJTU. In 2004, he worked as a visiting scholar in Nanyang Technological University. He was an Associate Professor with XJTU in 1996, and a Full Professor in 2004. Then he was employed as a supervisor of PhD student. He is also the associate Dean of the Faculty of Industry Automation. His research interests are power quality, active power filter, reactive power compensation, inverters for distributed power generation, etc. He is the author or coauthor of more than 120 papers was indexed by SCI and EI. He is the key finisher of four projects sponsored by National Natural Science Foundation of China, and more than 40 projects cooperated with companies from industry. He is the owner of four provincial and ministerial level science and technology advancement award. Professor Zhuo is a member of IEEE, China Electrotechnical Society and Power Supply Society.

Xiaokang Liu was born in Shaanxi Province, China, in 1991. He received the B.Sc. and M.Sc. degrees in electrical engineering from Xi'an Jiaotong University, Shaanxi, China, in 2013 and 2016, respectively. Since November 2017, he has been working toward the Ph.D. degree in electrical engineering in Politecnico di Milano, Italy. His research interests include power electronics modeling, electromagnetic compatibility modeling and signal integrity.



Zhao Xu (M'06-SM'13) received the Ph.D. degree in electrical engineering from The University of Queensland, Brisbane, Australia, in 2006.From 2006 to 2009, he was an Assistant and later Associate Professor with the Centre for Electric Technology, Technical University of Denmark, Lyngby, Denmark. In Feb 2010, He joined Department of Electrical Engineering, Hong Kong Polytechnic University (PolyU), as an Associate Professor and Leader of Smart Grid Research Area. He is now Professor and Director of Power System Laboratory with PolyU. His research interests include demand side, grid integration of wind power, electricity market planning and management, and AI applications. He has edited 1 book, and published over 100 technical papers in international top journals, and conferences. He is a Senior Member of IEEE, the Chairman of IEEE PES Joint Chapter and IEEE Hong Kong Section, and an Editor of the IEEE Transactions on Smart Grid and the IEEE Power Engineering Letters.

Yixin Zhu (S'11-M'17) received the B.S., M.S. and Ph.D. degrees in electrical engineering all from Xi'an Jiaotong University, Xian China, in 2009, 2011 and 2015, respectively. In 2016, he joined Jiangnan University as a Lecturer. He is currently with the School of IoT, Jiangnan University. His research interests include the design, control and application of the high-power active power filter, the photovoltaic grid-connected inverter, and also the modeling, analysis and power management of the micro-grid.