WDM-based Silicon Photonic Multi-Socket Interconnect Architecture with Automated Wavelength and Thermal Drift Compensation

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***Abstract*—A silicon photonic circuit comprising all the building blocks necessary to demonstrate optical communication between two sockets interconnected through an Arrayed Waveguide Grating Router is reported. The paper focuses on the robustness of the interconnection scheme to the unavoidable wavelength and thermal fluctuations observed in real datacenter environments. To improve the reliability of the system, a feedback control mechanism, based on ContactLess Integrated Photonic Probes and heater actuators, is added to the interconnection to monitor in parallel the working point of each sensitive device and keep it locked in real-time. Experimental results demonstrate successful operations in a $30\,\mathrm{Gbit/s}$ data routing scenario at $5 \cdot 10^{-11}$ bit error rate, irrespective of sudden wavelength shifts of up to $200\,\mathrm{pm}$ or of iterated thermal variations in a $10\,^{\circ}\mathrm{C}$ temperature range, with a recovery time of around $30\,\mathrm{ms}$. These results prove that AWGR-based interconnections equipped with real-time drift compensation systems can be a viable option in multi-socket layouts even in highly demanding environments.**

***Index Terms*—Silicon photonics, thermal drift compensation, CLIPP sensor, wavelength division multiplexing, AWGR-based interconnect**

I. Introduction

With the demand for data traffic capacity in intra datacenter applications roughly doubling every year [1], novel techniques must be developed to cope with traffic growth. Two key problems that arise when scaling up capacity are the increased power consumption of the processors and the latency in the communication between them. These problems have driven research interest on novel multi-socket-boards (MSB), that integrate several processor sockets on a single board interconnected with a low latency interface. Schemes as Intel's QPI [2] can offer glue-less interconnection but are limited to a maximum of 8 processors, while switch-based approaches like Bixby [3] can support a much larger number of processors but suffer from critical energy and latency restrictions.

A promising solution to overcome the radix-latency trade-off is found when using photonic integrated interconnections. In particular, optical architectures based on Arrayed Waveguide Grating Router (AWGR) have already been demonstrated to enable any-to-any, low-latency, low-energy communication even between more than 8 nodes [4]. Figure 1 shows the AWGR-based NxN static interconnection scheme recently proposed within the H2020 ICT-STREAMS European project [5]. Each processor is equipped with a transmission engine (Tx), featuring N-1 lasers at different wavelengths that are combined on a single bus by an optical (N-1):1 multiplexer (MUX) to produce WDM-encoded data streams. The carriers of each data stream get routed by the AWGR to different receivers depending on their wavelength, with collision-less transmission achieved thanks to the cyclic-frequency routing properties of the AWGR. At the receiving side (Rx) of each socket, the WDM-encoded data stream gets demultiplexed with a 1:(N-1) optical demultiplexer (DEMUX) so that each wavelength is acquired by a separate receiver, allowing to discriminate the transmission from each sender. In this way, every processor can simultaneously communicate with all the others by simply encoding its electrical information on the wavelength of the target receiver, allowing any-to-any direct interconnection without the need of switching mechanisms.

AWGRs have been demonstrated to be effective routing engines in any large integration scale platforms, including Silicon Photonics (SiP), Indium Phosphide and Silicon Nitride [6]–[9]. Silicon Photonics, the technological platform used in this work, enables in particular the largest integration scale and includes all the functional building blocks required by the proposed interconnection scheme [10]. However, as the number of components on a single chip grows, the requirements on their control become critical. The large sensitivity to fabrication parameters together with the high thermal coefficient of silicon prevent open-loop operations, requiring feedback stabilization to counteract any wavelength or thermal instability and safeguard the functionality of the system even in real datacenters environments. Thus, algorithms and strategies to tune, reconfigure, calibrate and operate such devices are needed to maintain the performance at the required levels [11]–[18].

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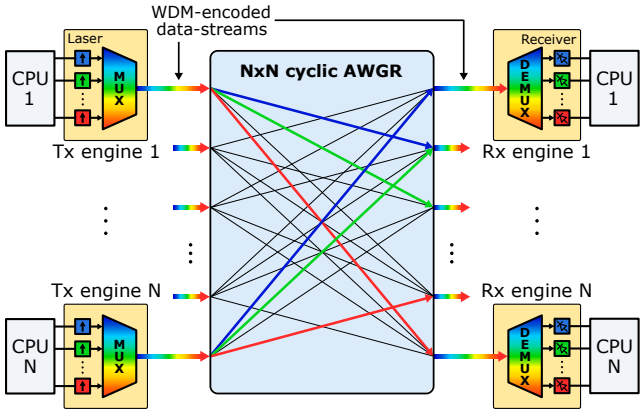

Fig. 1. CPU interconnection scheme proposed within the H2020 ICT-STREAMS European project. Thanks to WDM data encoding and to the cyclic-frequency routing properties of the NxN AWGR, any-to-any direct communication is possible even between more than 8 CPUs, without the need of switching mechanisms.

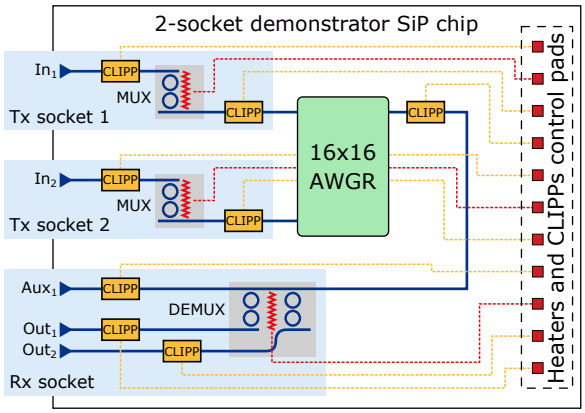

Fig. 2. Schematic view of the WDM-based Silicon Photonic two-socket interconnect architecture integrated in a single chip.

Most of the proposed control methods rely on the extraction and measurement of a small part of the light from the main optical path [19]. This solution becomes quickly unfeasible for high-density systems, where the insertion of many detectors causes an unacceptable drop of the overall optical power reaching the output. Non-invasive photodetectors are thus an attractive alternative, as they promise to solve the aforementioned issues and allow the control of large scale architectures. The work in [20] presents a microring based switch matrix, where the photoconductive effect of waveguide integrated heaters is exploited to monitor the amount of light inside each device. As a drawback, the waveguide doping that is required induces an additional optical loss due to the high quality factor of ring resonators that could impair high-density datacom applications. In [21], the control of a Mach-Zehnder interferometer optical switch is presented, exploiting the same heater photoconductive effect. However, a calibration of the system is needed to account for the dark current of the detectors, a time and resource consuming approach that might become unpractical as the number of sensors increases and in presence of external unpredictable temperature variations.

A possible alternative is represented by the ContactLess Integrated Photonic Probe (CLIPP), an in-line detector that performs truly non-invasive light monitoring. The sensor only exploits the intrinsic light-induced free carrier generation happening at the Si/SiO_2 interface and, since it does not require any direct contact to the core or additional doping, it does not induce any detectable change in the waveguide propagation losses [22]. The use of this detector has already been validated in add/drop ring resonators [23], silicon switch fabrics [24] and others, but not in multi-component WDM AWGR-based layouts. In this paper, we present a novel CLIPP-equipped AWGR-based dual-socket interconnect system, that includes an automated calibration-free feedback mechanism for tuning and locking the resonances of its constituent building blocks. The proposed interconnection scheme is equipped with a custom electronic platform to read the CLIPP sensors in the system and automatically control the working point of each photonic device in real-time, allowing to counteract any wavelength or temperature fluctuation to keep the operation of the architecture stable in time and improve its robustness. Experimental verifications reveal successful resonance locking of 3 cascaded photonic devices in the timescale of milliseconds while the performance of the interconnect system was assessed in a $30\,\mathrm{Gbit/s}$ non-return-to-zero (NRZ) routing scenario for both wavelength and temperature variations in a wide range ($0.9\,\mathrm{nm}$ and $10\,^{\circ}\mathrm{C}$ respectively). Error-free operation is achieved in all the tested conditions. The full functionality of the system is finally demonstrated, with two optical signals successfully routed through the AWGR based interconnect system with negligible performance degradation, confirming that the architecture can be effectively exploited even in systems with more than two sockets.

The paper is organized as follows: Sec. II provides a description of the complete system; Sec. III presents the control strategy; Sec. IV describes the experimental setup; experimental results are reported and discussed in Sec. V and VI, and finally the dual-socket operation is demonstrated in Sec. VII.

II. Overview of the Complete System

A. Photonic chip

To prove the advantages of feedback controlled stabilization in keeping the performance of the system at the required levels, a subsection of the proposed interconnection scheme was designed and integrated in IMEC's ISIPP50G platform in a single photonic chip featuring all the necessary building blocks to demonstrate optical communication between two transmitting sockets and a receiving one. Each Tx socket is here equipped with a single laser to simplify the complexity of the assembly, but the approach and the obtained results can be extended also to a multi-laser situation.

As depicted in Fig. 2, the demonstrator incorporates a 16x16 O-band DWDM AWGR [25], with a channel spacing of $1.1\,\mathrm{nm}$ and a free spectral range (FSR) of $17.6\,\mathrm{nm}$, allowing non-blocking communication of the two Tx socket through wavelength-based routing. Each socket is interconnected to the AWGR optical engine through a 8x1 MUX with an FSR of

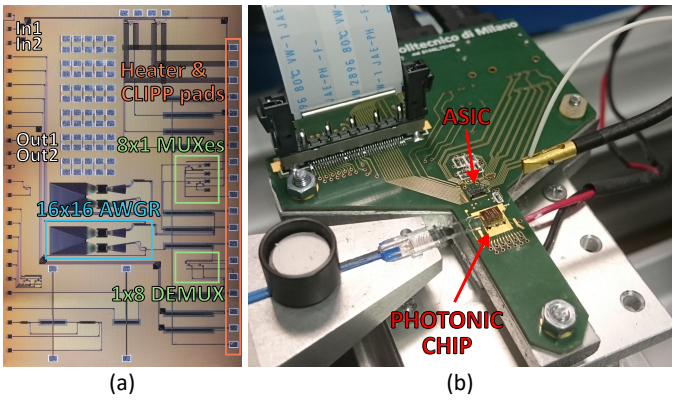

Fig. 3. (a) Picture of the photonic chip fabricated by IMEC and (b) chip-on-board assembly with the electronic ASIC and the cables to the FPGA-based control platform.

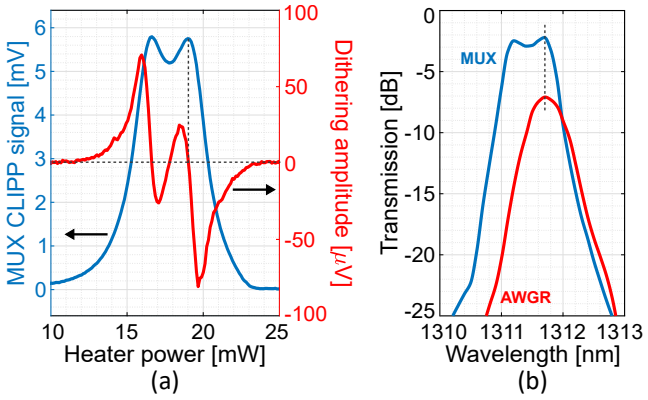

Fig. 4. (a) Measured MUX CLIPP signal and dithering amplitude as a function of the control heater power, highlighting the perfect alignment of the MUX peaks with the zero crossing points of the dithering signal. (b) Transfer function of the MUX locked to the AWGR response, showing an insertion loss of 2.2 dB and 7 dB respectively.

9.6 nm, based on cascaded double-ring resonators to provide sufficient selectivity and out-of-band attenuation and allow a very compact design with a low thermal tuning mechanism as compared to other implementations [26]. The AWGR combines the two input signals generated by the transmitters and routes them towards the receiver through a 1x8 DEMUX with a structure similar to the one employed for the MUX. The access to the optical inputs and outputs, denoted in figure as In_1, In_2, Out_1 and Out_2, is achieved via IMEC TE-polarization grating couplers (GC), all at the left side of the chip. Integrated heaters allow fine thermal tuning of the MUX and DEMUX resonances, while CLIPP sensors are employed to monitor the optical power in the system. Both the CLIPP sensors and the integrated heaters are accessible through electrical DC pads at the right side of the chip and are wire-bonded to the electronic board. A photograph of the chip is reported in Fig. 3(a).

B. Readout electronics & signal processing platform

The photonic chip is wire-bonded to a custom front-end CMOS ASIC, specifically designed for CLIPP readout and fabricated in 3.3 V 0.35 µm AMS CMOS process [27]. The ASIC features an ultra-low noise, 100 MHz bandwidth, capacitive-feedback trans-impedance amplifier, followed by 2 integrated double-balanced mixers that allow simultaneous in-phase and in-quadrature lock-in down-conversion of the CLIPP signals (typically around 1 MHz) to an intermediate frequency (around 20 kHz), well above the 1/f noise of the following stages, to facilitate cable transmission to the control platform. The use of an ASIC directly wire-bonded to the photonic chip allows to minimize the stray capacitances due to the connections and consequently maximize the signal-to-noise ratio (SNR) of the sensor readout, reaching a resolution of around 100 fS in the measurement of the waveguide conductance, corresponding to a sensitivity of around −35 dBm in the measurement of the optical power.

The photonic chip and the ASIC are mounted on a compact interface board, shown in Fig. 3(b), to facilitate optical coupling and electrical access to the CLIPP sensors and the integrated heaters. The board is equipped with a thermistor in order to monitor in real time the temperature of the photonic system, while a thermoelectric cooler (TEC) mounted right below the interface board allows tuning of the on-chip temperature. Both the thermistor and the TEC are connected to a TEC controller that allows temperature logging and generation of arbitrary on-chip thermal variations. The interface board is connected to a FPGA-based control platform [28] that A/D converts all the CLIPP signals, performs a parallel digital lock-in processing with selectable averaging times (from 8 µs to 25 ms), drives all the heaters in parallel and operates the most suitable strategy to achieve real-time closed-loop control of the architecture, providing reconfigurability and flexibility to the system.

III. Control Strategy

Several approaches have been proposed to lock the resonant wavelength of microring based structures, for instance by monitoring the output power level [29] or the bit-error rate of the optical signals [30]. The dithering technique [31] is here preferred, in order to achieve an easy yet effective true power and temperature independent locking of the rings. To do so, a small sinusoidal signal is added to the MUX and DEMUX heater voltages, thus modulating the light in the output waveguide. The resulting signal measured by the CLIPP is synchronously demodulated with a digital lock-in amplifier, obtaining, in this way, a voltage proportional to the first derivative of the transfer function of the device with respect to the temperature. Since the dithering signal is zero when the devices are tuned at resonance, this information can be used as error signal to lock the rings. This kind of set point is independent of the power circulating inside the ring, making the technique advantageous in situations where the input light power might fluctuate during operations. In addition, thanks to the anti-symmetric shape of the derivative signal, the position of the resonance is determined without ambiguity.

Fig. 4(a) shows the MUX transfer function and its dithering signal as a function of the heater power, measured with a CLIPP at the drop port of the filter. The application of a dithering modulation of 10 mV amplitude (corresponding to around 600 µW in terms of power) and 6 kHz frequency

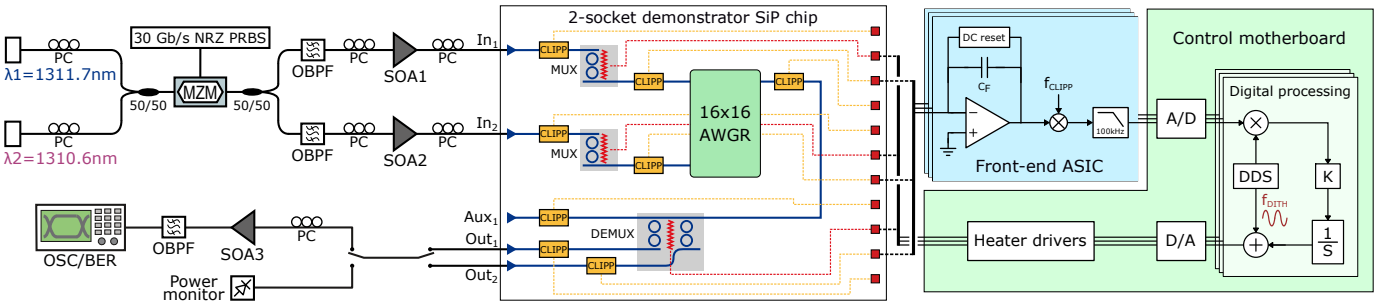

Fig. 5. Schematic of the experimental setup, showing the external laser sources, the SiP chip, the ASIC and the electronic platform.

allows to obtain a sufficiently high signal-to-noise ratio in the extraction of the derivative information, yet without affecting the quality of the transmitted signal [31]. The double peaked transfer function of the filter is due to a slight overcoupling of the rings, that can be solved by using two separated heaters to control them independently allowing also an improvement in terms of insertion loss. The use of a single collective heater was here preferred to simplify the control strategy while still allowing to match the MUX grid to the respective laser grid. Fig. 4(b) shows the spectral response of the ring-based multiplexer aligned to the AWGR response. It can be seen that the algorithm locks one of the two peaks, since it maximizes the power at the output of the MUX by minimizing the dithering signal.

The system architecture implemented to independently lock MUX and DEMUX, incorporating the CLIPP sensors and the integrated heater actuation is shown in Fig. 5. The first derivative of the transfer function, extracted with the lock-in technique described above, is used as the error signal of each control loop. The loops are completed by integral controllers, that drive the heaters to keep the devices at resonance. In this way, a robust and power independent feedback control is implemented. The bandwidth of each loop can be digitally tuned and has been set in the following experiment to $30\,\mathrm{Hz}$, to minimize the readout and actuation noise yet allowing a fast recovery time. Notice that, since the target of the feedback is to counteract wavelength and temperature fluctuations that are usually characterized by slow time evolutions in the seconds timescale, a $30\,\mathrm{Hz}$ bandwidth is large enough for this application.

IV. Experimental Setup

Fig. 5 shows the experimental setup used for the characterization of the presented photonic chip. The setup serves a dual purpose: i) the assessment of the CLIPP-based feedback stabilization system in various thermal and wavelength scenarios and ii) the evaluation of the system performance in terms of optical transmission quality for two optical data paths routed through the AWGR interconnect. To this end, two laser beams ($\lambda_1 = 1311.7\,\mathrm{nm}$, $\lambda_2 = 1310.6\,\mathrm{nm}$) were combined in a 50/50 optical coupler and injected into an O-band Mach-Zehnder Modulator (MZM). The two employed wavelengths correspond to the channels of the AWGR optical spectrum. A bit pattern generator (PRBS7-1) was used to generate a NRZ pseudo-random binary sequence at $30\,\mathrm{Gbit/s}$ with a peak amplitude of $300\,\mathrm{mV}$, that was then amplified by an SHF 807B high-speed RF driver amplifier to drive the MZM. The resulting modulated signals were split in a 50/50 optical coupler and filtered with a $0.5\,\mathrm{nm}$ $3\,\mathrm{dB}$ bandwidth optical band pass filter (OBPF), allowing the separation of the two wavelengths. Each resulting signal was amplified in a semiconductor optical amplifier (SOA1 and SOA2) to obtain an average optical power of around $10\,\mathrm{dBm}$ and then coupled to the input ports of the SiP chip through the corresponding GCs. The signals routed through the SiP chip were again coupled at the output with GCs. A third semiconductor optical amplifier (SOA3), electrically driven at $175\,\mathrm{mA}$, was used to provide an average gain of around 20 dB to compensate for the chip losses. In detail, the input and output GCs add an overall $10\,\mathrm{dB}$ of losses, the MUXes and the DEMUX around $2.2\,\mathrm{dB}$ each and the AWGR around $7\,\mathrm{dB}$, for a total attenuation of around $22\,\mathrm{dB}$. This number can be reduced to around $10\,\mathrm{dB}$ by choosing edge couplers, that are reported to have insertion loss lower than $0.5\,\mathrm{dB}$ [32], and by driving MUX and DEMUX with independent heaters on each ring. After amplification, the light was injected in another $0.5\,\mathrm{nm}$ $3\,\mathrm{dB}$ bandwidth optical bandpass filter, to filter out the SOA amplified spontaneous emission (ASE). Finally, the two signals were monitored with a sampling real-time oscilloscope (RTO) and evaluated in a Bit Error Rate Tester (BERT). Polarization controllers (PC) were employed throughout the experimental setup to ensure operation at the optimal polarization for both the SOAs and the GCs.

V. System Robustness vs Wavelength Shifts

A. Automatic locking and recovery

The performance of the implemented closed-loop control was first evaluated in terms of capability to react to wavelength variations. To this aim, a single input laser, the MUX, AWGR and the DEMUX were first tuned and locked to maximize the output power. The optimal operating point of the system was then intentionally perturbed by shifting the laser wavelength with a step of $200\,\mathrm{pm}$. Fig. 6 shows the time evolution of the optical power at the output of the chip, measured with an external photodiode in four different scenarios.

The first experiment was conducted in open loop, i.e. with no control action, by applying a positive wavelength shift. As shown in the curve "NOT-locked (+200 pm)", a loss of about $6\,\mathrm{dB}$ was measured at the output of the system, since after

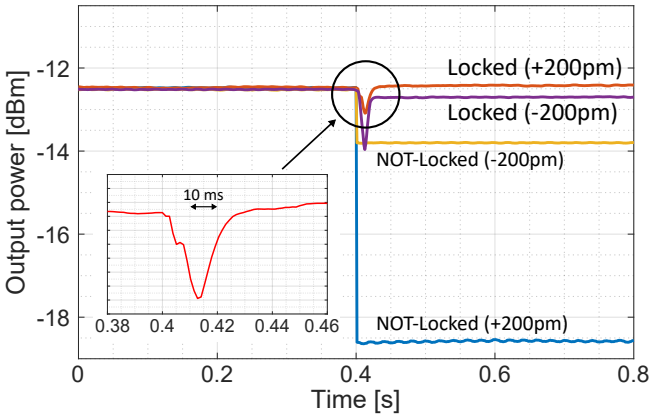

Fig. 6. Time evolution of the power at the output of the chip when perturbing the laser wavelength with $\pm 200\,\mathrm{pm}$ steps. The comparison between locked and not locked situations is reported. The closed loop transient response is expanded in the inlet, showing a fast recovery time of about $30\,\mathrm{ms}$.

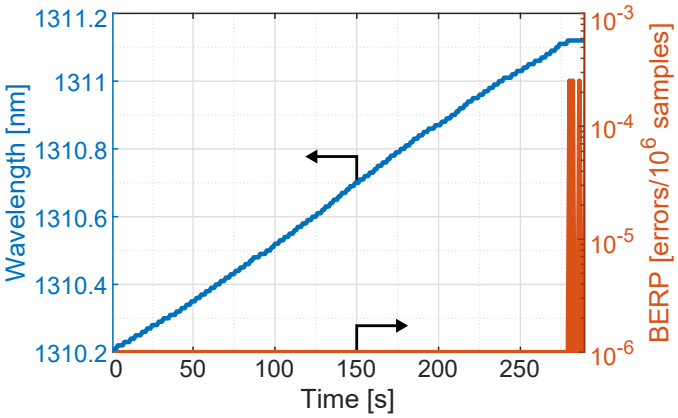

Fig. 7. Wavelength sweep and recorded BER per acquisition (10^{-6} bits long sequences) obtained with the RTO. The control loop successfully tracks the shift to ensure error-free transmission on the full passband of the AWGR.

the step the laser is outside the MUX and DEMUX passband. A second experiment was then conducted with the control of MUX and DEMUX activated in real time. The curve "Locked (+200 pm)" shows how the system is able to swiftly recover its working point after the wavelength detuning. The final power level is slightly different from the initial one because of the not perfectly flat response of the AWGR in its passband (Fig. 4(b)). The inlet of Fig. 6 expands the transient of the experiment, allowing to estimate a recovery time of the system of around $30\,\mathrm{ms}$, coherently with the selected bandwidth of the control loop being $30\,\mathrm{Hz}$. Notice that this is not the switching time of the network, since the static topology doesn't require any reconfiguration during its operations. Instead, it should be considered as the maximum transitory time to recover from abrupt variations of the optimal working point and as the initial tuning time needed to configure the system at start-up.

A similar experiment was conducted from the same starting point by shifting the input laser wavelength with a -200 pm step. Fig. 6 also shows these results, in which a steady loss of about $3\,\mathrm{dB}$ is measured when the system is operated in open-loop. The loss is different than before because MUX, DEMUX and AWGR are now operating in different working points with respect to the previous experiment. Also in this case, the system realigns both MUX and DEMUX in real-time to the new signal wavelength within the $30\,\mathrm{ms}$ of the closed loop response time.

B. BER assessment

The effectiveness of the real-time control loops of MUX and DEMUX in counteracting wavelength shifts has also been assessed by acquiring the BER at the output of the system. To this aim, a single modulated signal was injected in the chip and a real-time oscilloscope (RTO) was used to track the output. The instrument performs BER evaluation by comparing the bit pattern coming from the chip with the expected bit sequence. The measurement is performed on 10^6 long bit sequences, leading to a minimum obtainable BER of 10^{-6}. For this experiment, the wavelength of the input laser was manually ramped from the starting value of $1310.2\,\mathrm{nm}$ up to $1311.1\,\mathrm{nm}$, with steps of $10\,\mathrm{pm}$, as shown in Fig. 7. The closed-loop control was kept always active, in order to safeguard the MUX and DEMUX resonance during the whole sweep. Indeed, the figure shows that the transmission stays error-free (BER below 10^{-6}) along all the passband of the AWGR. Only when the input laser falls outside the AWGR window the output power drops significantly and the BER increases, even though the MUX and the DEMUX are still well tuned.

VI. Thermal Drift Compensation

In real datacenter environments, temperature instabilities are one of the main issues to be faced when employing Silicon Photonics devices. Consequently, the proposed optical interconnection scheme was also tested in a temperature unstable scenario, to demonstrate that a closed-loop control can effectively compensate thermal drifts in real time. To this aim, temperature oscillations were intentionally generated in the setup, using the aforementioned TEC controller. Fig. 8(a) shows the temperature profile recorded during the 20 minutes long experiment. The average value of the temperature was slowly swept between $25\,^{\circ}\mathrm{C}$ and $35\,^{\circ}\mathrm{C}$, with sinusoidal oscillations superimposed to it to simulate faster fluctuations. A single $30\,\mathrm{Gbit/s}$ modulated laser signal was injected into the system and monitored at the output to obtain both eye diagrams and BER measurements, while a second laser served as a continuous wave crosstalk source.

Fig. 8(b) and (c) show the temporal evolution of the MUX and DEMUX heater voltages, generated by the feedback loop during the experiment. They mirror very precisely the temperature variations, confirming that the locking action is able to effectively compensate the external thermal drifts. This is also proved by the transmission quality measurements performed on the output signal. The BER measurements at the BERT and eye diagrams captured with the RTO are reported in Fig. 9. Error-free operation at $5 \cdot 10^{-11}$ error-rate was obtained during all the 20 minutes of the experiment and within $10\,^{\circ}\mathrm{C}$ temperature range, with a power penalty variation of $0.3\,\mathrm{dB}$ due to the not actively controlled AWGR response and a maximum power penalty of around $1\,\mathrm{dB}$ when compared to the input signal (BtB). In addition, the crosstalk effect

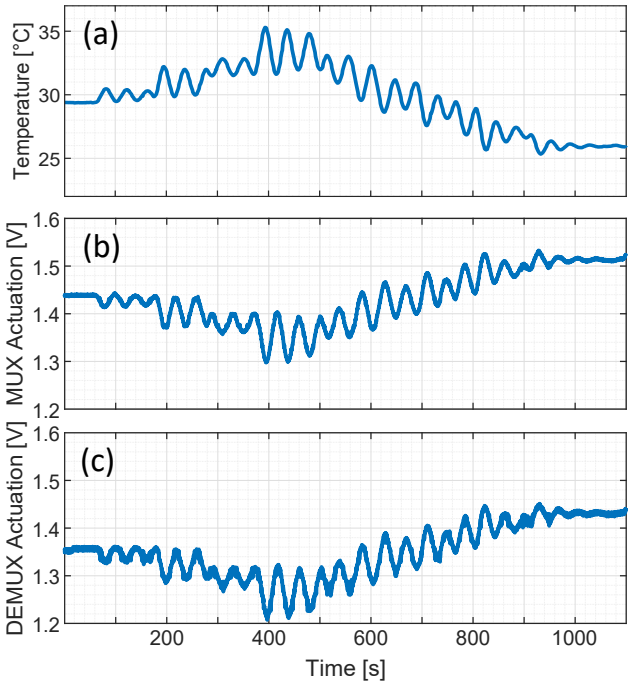

Fig. 8. (a) Temperature variations imposed to the chip during the experiment with a Peltier cell and actuation voltage of (b) MUX and (c) DEMUX heaters, generated by the control loop. Notice how the control action on the actuation voltage mirrors perfectly the external temperature variations.

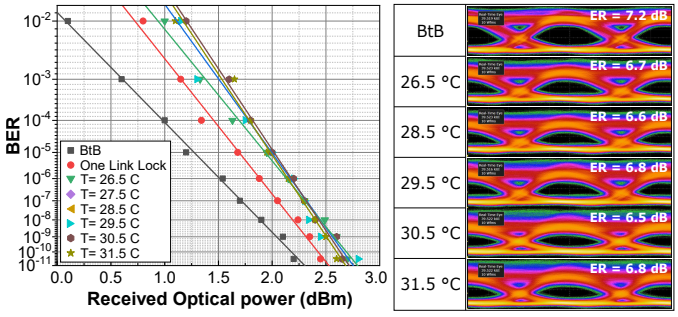

Fig. 9. BER measurements and eye diagrams at $30\,\mathrm{Gbit/s}$ acquired at different temperatures. The thermal variations are successfully compensated and the transmission quality is preserved.

induced by the second optical signal resulted to be negligible on the transmission quality (power penalty lower than $0.4\,\mathrm{dB}$). The same is confirmed by the eye diagrams, that retain an extinction ratio (ER) larger than $6.5\,\mathrm{dB}$ in all the explored conditions.

VII. Demonstration of Dual-Socket Operation

After having successfully evaluated the performance of the CLIPP-enhanced AWGR-based interconnect for one modulated optical input in various unstable conditions, the full functionality of the 2-socket architecture was assessed. To this end, two input lasers (at $\lambda_1 = 1311.7\,\mathrm{nm}$ and $\lambda_2 = 1310.6\,\mathrm{nm}$ respectively, modulated at $30\,\mathrm{Gbit/s}$) were injected to the chip ports In_1 and In_2. The two MUXes were automatically tuned to route the light to the AWGR inputs, with both signals emerging from the same AWGR output port. The two wavelengths were demultiplexed again with the DEMUX and the resulting output

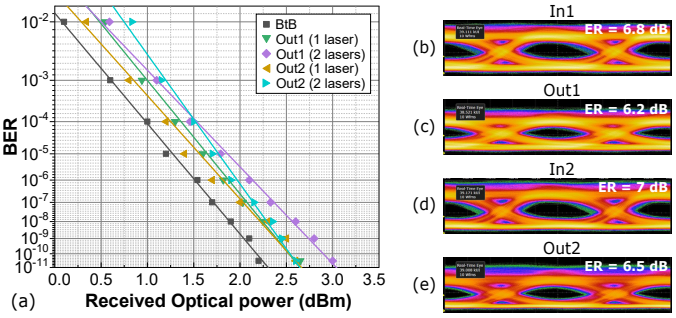

Fig. 10. (a) BER measurements and (b), (c), (d), (e) eye diagrams obtained when routing two $30\,\mathrm{Gbit/s}$ signals through the interconnect system. The crosstalk between two channels causes a negligible $0.5\,\mathrm{dB}$ power penalty.

signals were monitored to assess the quality of the interconnection. This experiment therefore required the simultaneous locking of the 3 resonant photonic components. Fig. 10 shows the acquired optical eye diagrams and BER measurements of the full 2-socket system, as compared to the case when only one socket is operated. In particular, Fig. 10(b) and (d) show the eye diagrams of the signals that were injected to the chip, featuring an ER of $6.8\,\mathrm{dB}$ and $7\,\mathrm{dB}$ respectively. Fig. 10(c) and (e) show the corresponding eye diagrams of the two DEMUX outputs. Both outputs retain clearly open eyes, with only a slight deterioration in the ER ($6.2\,\mathrm{dB}$ and $6.5\,\mathrm{dB}$ respectively). The origin of this degradation is to be found in the SOA induced pattern effect, while the optical crosstalk was observed to have a low impact, measured around -21 dB. The result is confirmed by the BER measurement. Fig. 10(a) shows the acquired BER measurements when one or both optical signals are enabled. The measurements reveal a negligible power penalty of $0.5\,\mathrm{dB}$ when both optical signals are routed through the AWGR interconnect and all the photonic components are locked with the CLIPP system as compared to the single optical path case, confirming the successful operation of the architecture.

VIII. Conclusions

In this paper, a novel silicon photonic AWGR-based interconnect architecture for optical communication between two CPU sockets was presented and discussed. The work wanted to demonstrate the mitigation of the very high sensitivity of these structures to temperature and wavelength variations, that is a big challenge to be faced when these devices are to be used in unstable environments, such as datacenters. To this aim, the addition of an automated drift compensation system, based on CLIPP sensors and integrated heaters in multiple real-time control loops, was proposed and experimentally demonstrated to safeguard the resonance of the sensitive building blocks of the interconnection scheme. The eye diagrams and BER measurements on the outputs confirmed that the presented solution ensures high quality optical transmission in a wide range of wavelengths and temperatures, with negligible power penalties. The dual socket operation of the interconnection was finally demonstrated, proving that the system can be successfully used in multi-socket architectures, even in demanding and unstable environments. The approach proposed in this

work can be extended also to other kind of detectors and interconnection topologies. When switching mechanisms are required, as in [33] and [34], feedback stabilization could be envisioned in combinations with look-up tables to enable both fast reconfiguration and good reliability against working point fluctuations.

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