Automatic Tuning of Silicon Photonics Microring Filter Array for Hitless Reconfigurable Add-Drop

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Abstract—Given the escalation of demand for high speed data interconnection, both between users and datacenters, high capacity optical networks need a boost in capacity, flexibility and efficiency. To stand up for those problems, the network reconfigurability is a key feature in a saturated and power hungry network operating scenario. In this paper, a reconfigurable optical node, using a commercial integrated photonics foundry was conceived, fabricated and tested. A novel application of automatic control of complex optical circuits involving locking and tuning of microring resonators is presented. The technique exploits a channel labeling strategy to identify a single optical channel amid a Dense Wavelength Division Multiplexing (DWDM) comb. The fabricated filter array provided add-drop ports with hitless channel reconfiguration and telecom graded specifications as $20\,\mathrm{dB}$ **of in-band isolation,** $40\,\mathrm{GHz}$ **of channel bandwidth in a microring filter with** $1\,\mathrm{THz}$ **of Free Spectral Range (FSR).**

Index Terms—Photonic Integrated Circutis, Silicon Photonics, Ring Resonators, Optical Add Drop, Hitless Filters.

I. INTRODUCTION

WHEN DWDM technology was introduced in optical transport networks, its main function was to provide capacity enhancement to point-to-point optical links. Thus, the only function needed was wavelength multiplexing and demultiplexing at each optical node [1]. With the advances in optical technology in the early 21st century, practical reconfigurable optical networks emerged. These networks make use of wavelength switching devices that can be dynamically configured to route a set of wavelengths between optical ports. The use of such reconfigurable optical devices together with wide bandwidth optical amplifiers [2], low loss optical fibers, and optical dispersion compensation fibers allowed the reach and capacity of optical transport networks to grew steadily for the last three decades [3]. The question that now is posed is what are the technologies that can cope with the growth in the bandwidth requirements imposed by services like 5G, Augmented Reality, Virtual Reality and all the machine-to-machine traffic that keeps growing. The technology that is most widespread and in use today, discrete photonics, does not address those requirements in a scalable and cost efficient way. Integrated Photonics and the generic foundry approach are the state-of-the-art technology that permits such evolution.

As the complexity of Photonic Integrated Circuits (PICs) grows, the requirements on control techniques become notorious. Algorithms and strategies to tune, reconfigure, calibrate

and operate such devices need to cope with thermal crosstalk, fabrication tolerances and environmental conditions in order to maintain the device performance in the required levels. To date, control techniques were already demonstrated to drive complex PICs such as 8x8 switch matrices [4], binary trees of Mach-Zehnder interferometers [5], to control add-drop ring filters [6], to lock ring modulators [7], [8] and many others. The work in [9] presents a control of silicon microrings based on the indirect measurement of the power inside the rings. As a drawback, the ring waveguide doping that is required to measure this intensity induces an additional optical loss that could be a problem for high density telecom applications. To solve that issue, the work in [10] reports the automatic tuning of a single Microring Resonator (MRR) using the Thermal Eigenmode Decomposition (TED) technique as in [11].

In this work, a reconfigurable optical node based on a Silicon Photonics (SiP) PIC was conceived, fabricated and tested, using a generic and commercial integrated photonics foundry. The proper design and analysis of a reconfigurable photonic integrated circuit system composed of an array of third order MRRs as shown in Fig. 1 is detailed and presented. The control strategy developed to keep the photonics in place is proposed and analyzed. The successful implementation of advanced control and reconfiguration functionalities of a complex and large-scale PIC are demonstrated. Although several works as [4]–[9] have addressed the problem of control in SiP, most of these have focused on single components or simple circuits with few components. The functional behavior of adding and dropping a data transmitting channel without affecting already established channels is, to the best of our knowledge, for the first time demonstrated in a SiP system.

This paper is organized as follows, in section II the design of a controllable telecom graded MRR based reconfigurable optical filter is presented, in section III the required control hardware and algorithm the filter array is demonstrated, in section IV the characterization of the individual filters and the demonstration of the hitless reconfiguration is shown, and finally in section V we present our conclusions.

II. DESIGN OF MICRORING FILTER ARRAY

The MRR filtering structure is the key element of the reconfigurable add-drop device. The first step in its design is the analysis of the required filter order to fulfill the requirements of telecom networks. One must check the necessary filter order that permits those specifications to be satisfied, and as a trade off, one must limit the control complexity that the

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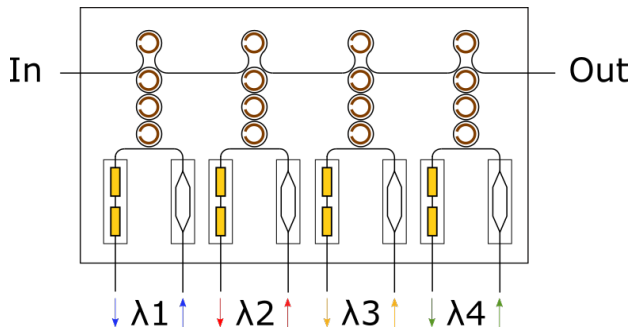
Fig. 1. Scheme of a 4 channel microring hitless based filter array where the add ports embed a Mach-Zehnder modulator to add a channel label and the drop ports have a transparent power monitor to distinguish individual channel powers.
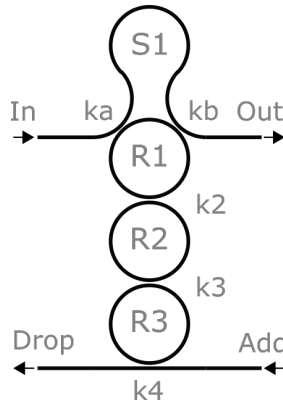

Fig. 2. Third Order MRR filter for tunable coupler detuning hitless strategy.

optical circuit will require. The design of such filter consists on the choice of the coupling coefficients between the resonating structures, using a specific synthesis strategy [12].

A. Filter synthesis

The order of the filter determines, among other things, how steep its transfer function can be and its the chromatic dispersion. Higher the order, higher the maximum chromatic dispersion that the filter imposes to the signal and steeper the transfer function.

Two 3rd order MRR designs are compared in Fig. 3, one is designed using Butterworth design and another with Chebshev filter coefficients. The transfer functions are very similar, Chebyshev has a steeper roll-off resulting in a higher drop-port isolation at $50\,\mathrm{GHz}$ and $100\,\mathrm{GHz}$, but has a higher chromatic dispersion peak with respect to Butterworth as shown in Fig. 3b.By considering waveguides with group index $n_g = 4.202$, the required ring length to provide a FSR of $1\,\mathrm{THz}$ is $71.35\,\mu\mathrm{m}$, which was designed with a ring radius of $11.35\,\mu\mathrm{m}$.

The filter was designed considering the architecture shown in Fig. 2. The directional couplers power coupling coefficients (k_i) values were obtained with the synthesis strategy defined in [12], and for the Butterworth case the obtained values are $k_1 = k_4 = 0.233$, $k_2 = k_3 = 0.009$. In this case, the value for k_1 will be determined by the Mach-Zehnder (MZ)

based tunable coupler on the top coupler, that is given by the maximum power at the cross port of a Mach-Zehnder Inteferometer (MZI). Such value, as shown in [13], is given by

$$k_a = k_b = \sin^2\left(\frac{\arcsin(\sqrt{k_1})}{2}\right). \qquad (1)$$

Thus, $k_a = k_b = 0.062$. One should note that since these couplers have a small coupling ratio, the ripple on the bar state is also very small (less than 1 dB). Thus, the hitless operation is guaranteed.

B. Hitless architecture

Now that the filtering order and coefficients are defined, one must solve the issue of the impact on other channels, since the traditional tuning of coupled MRR filters naturally affects other channels in the through port. Thus, an intelligent filtering structure and strategy should be developed to make the tuning of coupled MRR filters truly hitless, *i.e.* not interfering with other channels. The most promising hitless architecture that were identified were already proposed by M. Popovic [14] and L. Bolla [15].Their main problems are the complexity of the control technique able to drive it in a DWDM environment. Our proposed architecture is the one shown in Fig. 2, in which there is only one tunable coupler responsible for the hitless feature, and the control is made possible by the direct access of the added signal at the drop port.

The detuning strategy is based on the single tunable input coupler in the MRR, labeled as S_1 in Fig. 2. With this scheme the filter can be disconnected at the In-Out port, while it can be accessed, tuned, controlled and locked from the Add-Drop port. A detailed strategy of tuning and locking is discussed in section III and the hitless tuning is guaranteed. Due to geometrical constraints, the two arms of the MZI implementing the tunable coupler cannot have the same length; the tunable coupler can be conveniently designed to have a FSR equal to the one of the MRR. Given this constraint, the tuning of the tunable coupler during the tuning of the reconfigurable add-drop must be done simultaneously with the tuning of the three MRRs. The hitless operation consists of inducing an unbalance in the MZI that realizes the tunable coupler to isolate the ring filter. In this way all the light entering in the In port is directed to the Out port.

The operation in such condition is shown in Fig. 4. In Fig. 4a it is shown the spectral response during the tuning phases, and in Fig. 4b the control signals applied to each one of the heaters is presented. With this strategy the neighbor channel is not affected by the reconfiguration of the filter, thus indicating a good solution for the hitless operation.

C. Hitless filter array

By cascading the wavelength filtering unities one can construct an array of filters to work as a multi-channel reconfigurable add-drop. An schematic of such structure is seen in Fig. 1. When designing such an array, one must take into account the effects of the cascading on the final performance of the individual filters. During operation, a particular attention
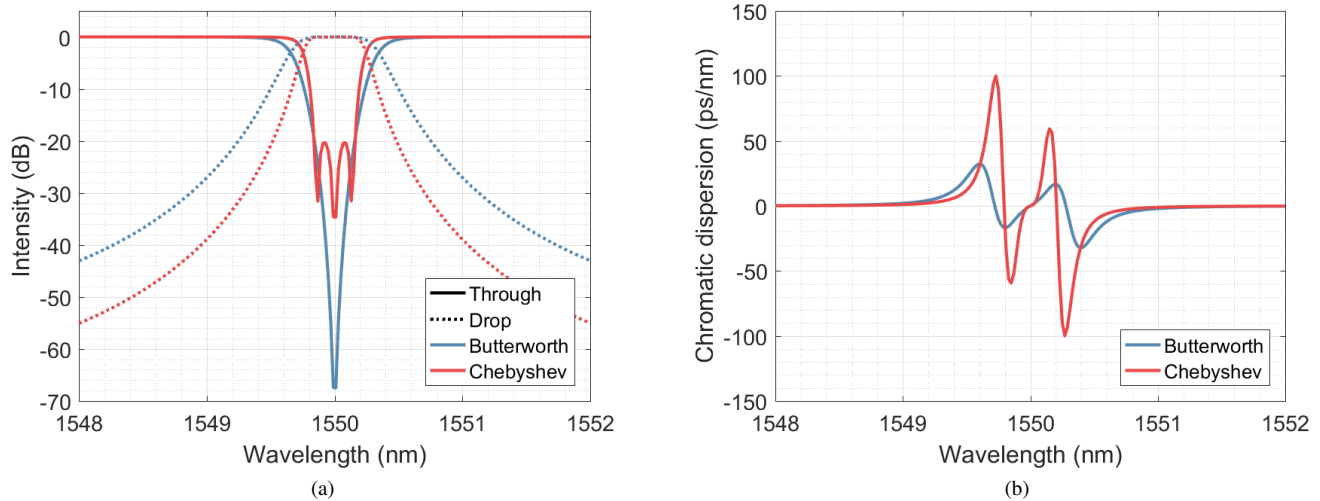
Fig. 3. Third order MRR designs comparing Butterworth and Chebyshev a) spectral profiles and b) chromatic dispersion
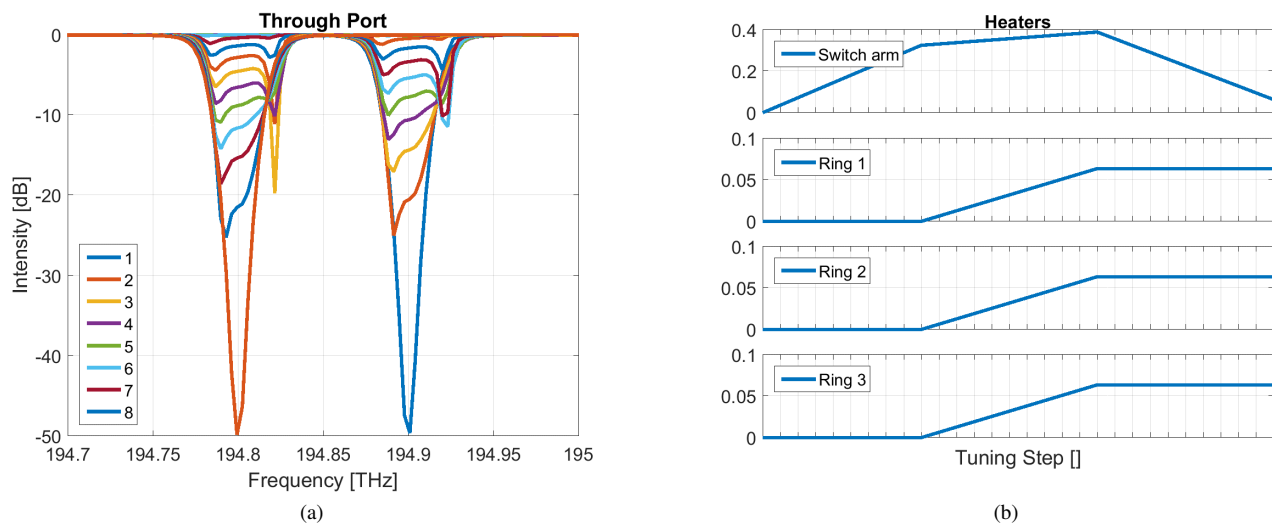

Fig. 4. a) Through port spectrum during the tuning in the Tunable Coupler detuning hitless scheme. b)Time evolution of the control values for the Tunable Coupler detuning scheme.

should be taken regarding thermal crosstalk that might affect the tuning of the individual filters.

Simulation results of the cascaded filter operation are shown in Fig. 8. There, it is possible to see that no significant effect on the through port is visible when connecting and disconnecting the filter from the bus. It should also be noted that the order in which the filters are tuned influences the overall behavior of the channels. It can be seen that the green curve, that in the simulation refers to the second add/drop port, suffers the influence of the first drop, red curve, on the left side of its low loss spectrum.

D. Channel labeling

To measure channel powers independently of either multiple optical signals or optical noise propagating simultaneously in a waveguide, one can combine the use of channel labeling and ContactLess Integrated Photonic Probe (CLIPP) [16] detectors.

To this aim, on the transmitter side, the channel is intensity modulated with a frequency f_q below the reading frequency of the CLIPP [17]. To not degrade the performance of the transmitted channel, a low modulation index μ ($< 8\%$) can be used [18]. This can be achieved with a MZ modulator driven with an amplitude much smaller than its V_π. The signal labeling can be performed either directly on-chip, by using thermally tuned MZ modulators [17] or with external modulators close to the transmitter.

To obtain the label power measurement one needs to add a label demodulation stage after the output of the CLIPP demodulator. The output signal of this second lock-in demodulator is proportional to the change in the waveguide conductance ΔG_{label} which is due to the labeled signal. Since the label is simply an amplitude modulation of the signal, the relation between the signal power and the label amplitude is given by the modulation index μ.
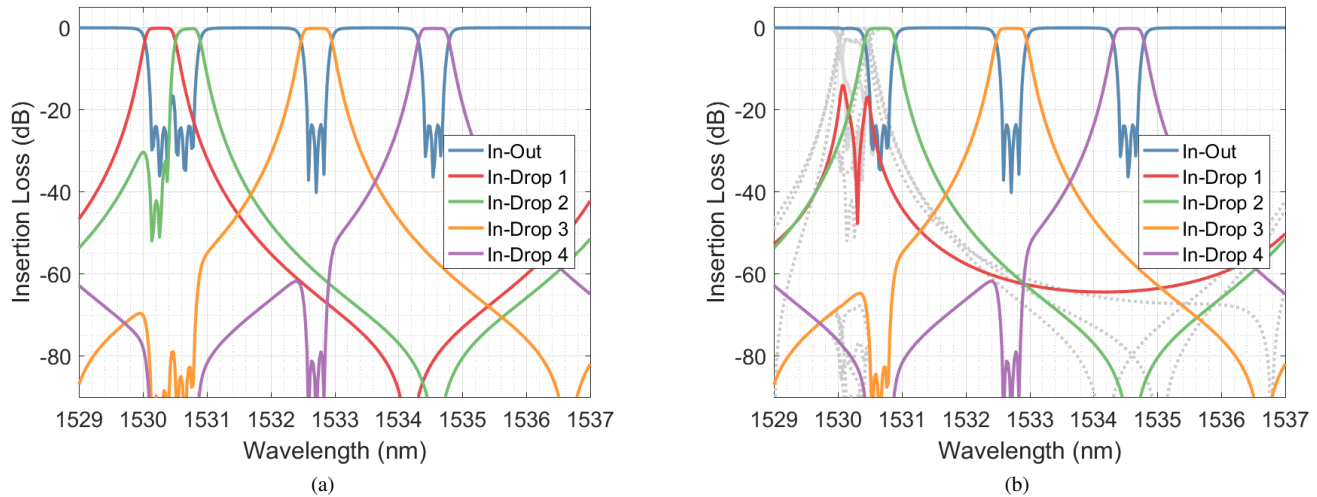
Fig. 5. a) Transfer function all output ports in which all filters are connected to the bus, each one at one channel. b) Disconnecting of one filter from the bus. In gray are shown the intermediate steps during the tunable coupler detuning process.

The penalty induced by the label is evaluated by a measurement of the Q factor from a 10 Gbps On-Off Keying (OOK) as a function of the modulation index μ. Figure 6 shows such measurement in which it is seen that when the intensity of the label increases, the penalty in the Q factor also increases. The two eye diagrams shown in the insets correspond to the label-free signal (Q = 7.7 dBQ) and to a label amplitude μ 19% (Q = 6.0 dBQ).

The sensitivity of the label measurement increases with both the modulation depth and the reduction of the electrical bandwidth of the measurement. As the reading speed increases, i.e. using wider read-out bandwidths, the sensitivity decreases. Thus one can also plan an adaptive reading of the CLIPP during the tuning, fast when the optical power is high and then slow down as the locking condition is reached. The same functionality can be achieved by using standard photodetectors and a suitable demodulation stage.

Fig. 6. Measurement of the Q factor penalty due to the insertion of a label on a 10 Gbps OOK signal.

III. CONTROL ARCHITECTURE

In this section a telecommunication graded hitless filter architecture is presented and its control technique detailed. An automatic algorithm is used to tune and lock the filtering unit to the channel to be added to a DWDM link. The functional diagram of the filtering unit is shown in Fig. 7a and a microphotograph if the fabricated filter is shown in Fig. 7b.

A. Control hardware

The PIC to be controlled needs sensors that detect the intensity of the light flowing in the waveguides in some key points through some physical effect to help the control unit, an electronic circuit, to understand the working point of the photonic circuit. Based on such information and the desired functional requirements, the control unit, both electronics and software, provides to the actuators the signals to steer the PIC towards the correct state.
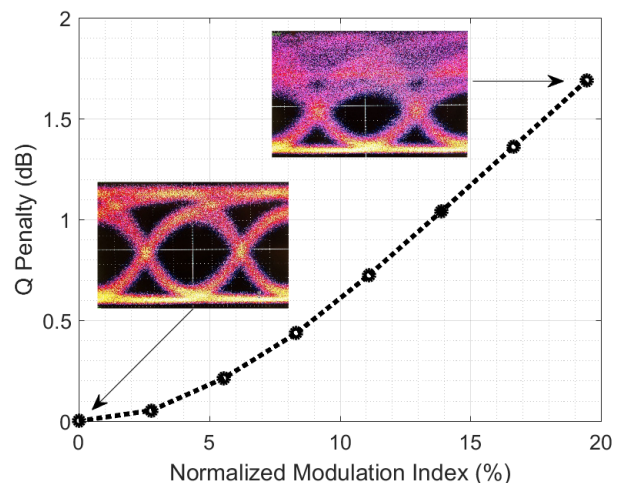
A representation of this concept in the scenario of the reconfigurable add-drop device is shown in Fig. 8b. The electronic controlling board called motherboard contains all the circuitry to drive the heaters, all the CLIPP readout circuitry and a Field Programmable Gate Array (FPGA) controller responsible, among other things, of performing the label demodulation of the control signals, as presented in sec. II-D. An image of the packaged photonic board and PIC is shown in Fig. 8a.

The CLIPP sensor is used as sensing element to detect the light intensity in the waveguide. The sensor measures the conductance of the waveguide core, that is proportional to the light power [16]. The lock-in technique is used as detection scheme: the waveguide core is accessed capacitively with the electrodes of the sensor, placed far enough from the waveguide to avoid any perturbation in the light electric field and stimulated with a sinusoidal signal. The generated current
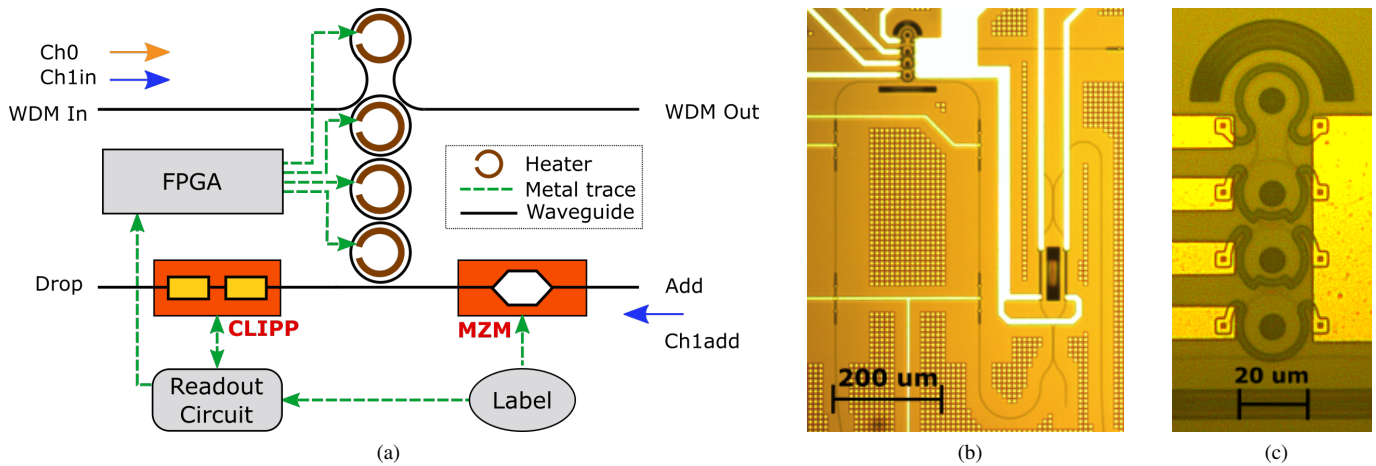
Fig. 7. a) Functional block diagram of the reconfigurable hitless filter. b) Filtering unit including monitoring CLIPPs and on-chip MZI to add label of add signal and c) hitless third order microring resonator filter with deep trenches to improve heater efficiency and reduce thermal crosstalk.
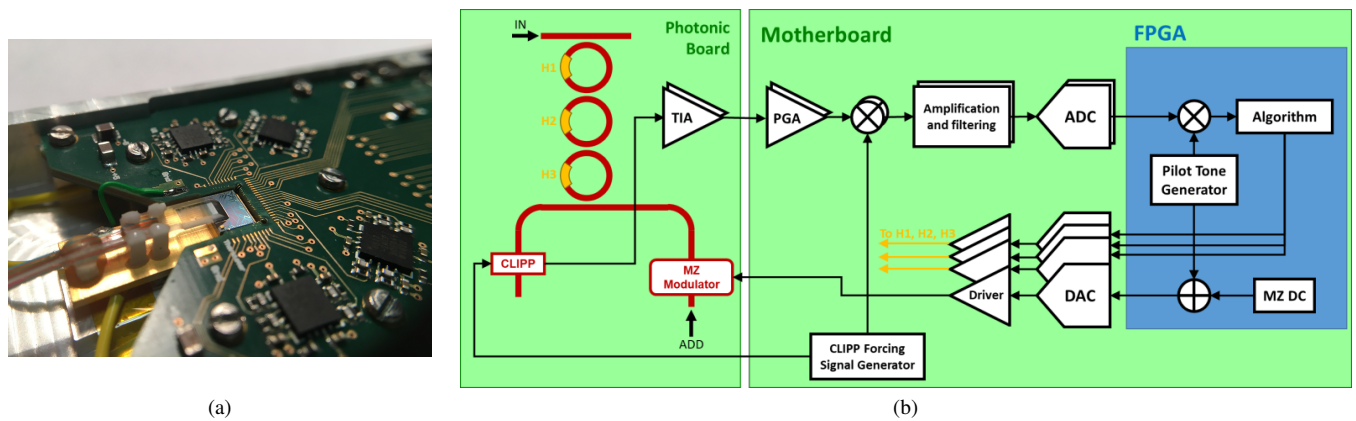

Fig. 8. a) Packaged Silicon Photonics chip and control electronics. Optical transposer to couple external optical fibers to on-chip gratings also shown. b) Schematic diagram depicting the control electronics around the photonic circuit.

is then collected, amplified and demodulated to extract the useful information. Low-noise readout is needed to reach a sufficiently high light sensitivity.

The electronic control hardware is designed as a modular structure, to achieve both easy optical packaging and high electronic performance. A first compact PCB, named Photonic Board, on the left of Fig. 8b, hosts the photonic chip, that is directly wire-bonded to the front-end Trans-Impedance Amplifier (TIA). To achieve low-noise and wide bandwidth, a ADA4817 amplifier with capacitive feedback (CF = 0.5 pF) has been chosen. A $100\,\mathrm{M\Omega}$ resistor in parallel to the capacitor allows to discharge the DC leakage currents. The TIA features $40\,\mathrm{MHz}$ closed-loop bandwidth and $60\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ output noise voltage power spectral density at $1\,\mathrm{MHz}$, making it well suitable for the application. The low noise performance reflects into a resolution in the measurement of the conductance of the waveguide of approximately $20\,\mathrm{ps}$ with a bandwidth of $10\,\mathrm{Hz}$, equivalent to a sensitivity around $-30\,\mathrm{dBm}$ in the optical power.

The Photonic Board is connected to the main Motherboard through a commercial CFP2 connector. The Motherboard is designed to: 1) generate the sinusoidal signal necessary to

stimulate the CLIPP; 2) Read in parallel up to 8 CLIPP sensors outputs; 3) Perform the control algorithms for tuning and locking of the working points of the photonic devices; 4) Drive the heaters (up to 24 in parallel) on the photonic chip to close the feedback.

The sinusoid to stimulate the CLIPP is synthesized with a AD9958 direct digital synthesizer (DDS) and fed to the CLIPP with a THS3001 driver. The frequency of the generated sinusoid ranges from $50\,\mathrm{kHz}$ to $10\,\mathrm{MHz}$ to adapt to different sensor geometries, while the amplitude of the signal can be chosen from $1\,\mathrm{V}$ to $10\,\mathrm{V}$ to maximize the signal-to-noise ratio of the measurement in all possible conditions. A second channel of the DDS generates the sinusoidal reference that is used to demodulate the CLIPP output.

The conditioning and acquisition of the signals from the Photonic Board is performed by a low noise chain (replicated 8 times). A gain stage (AD8008) allows to further amplify the signal coming from the TIA, to make the noise of the following stages negligible. The gain of each channel can be tuned to fully exploit the input voltage range of the AD835 analog multiplier, that is used to demodulate the CLIPP output to bring at low frequency the pilot tone information superimposed

to it. By choosing the pilot tone frequency properly (around $10\,\text{kHz}$), it is possible to keep the signal above the $1/f$ noise corner frequency of the acquisition chain after this first demodulation, thus not losing resolution in the measurement. An active anti-aliasing filter (LTC1562), a programmable gain amplifier (PGA281) and a 16-bit 1 MSps ADC (AD7903) complete the acquisition chain.

The control signals for the thermal actuators, set by the FPGA control algorithm, are generated by three 8-channels 16-bit DACs (LTC2656) and then buffered (AD8024) to provide the power to suitably drive the heaters with resistances of some hundreds of Ohms, and allow a maximum current levels of $50\,\text{mA}$. A voltage accuracy of around $1\,\text{mV}$ is required, so the bandwidth of the chain has been limited to $60\,\text{kHz}$, to be able to generate the $10\,\text{kHz}$ pilot tone while keeping low the noise level. 24 parallel chains are present, to drive up to 24 heaters or to drive 20 heaters and send 4 signals to external modulators for pilot tone labeling.

The digital core of the platform is a Xilinx Spartan-6 FPGA for versatile, real-time parallel processing. The FPGA is mounted on a commercial module (Opal Kelly XEM6310), including the necessary components to interface it with a PC running a custom C# control software via USB. The label sinusoid is generated with an internal DDS and then added to the DC bias of the MZ modulators. The same sinusoid is exploited by a set of digital lock-in demodulators to efficiently detect the pilot tones from the ADC acquisition. The waveguide power measurement is recovered after low-pass filtering of the demodulated signals with tunable IIR low-pass filters with bandwidth from $10\,\text{Hz}$ to $10\,\text{kHz}$. Based on the acquired information, the control algorithm is able to correctly set the voltage to be applied to the heaters and to lock the optical filter to the correct wavelength as described in the next section.

B. Control algorithm

The process of changing the channel needs to be hitless, meaning there should be no significant effect on other channels traveling in the bus waveguide, from In to Out port in Fig. 2, while channels are being changed. As discussed in Sec. II-B, to achieve this we need to disconnect the filter from the main bus. From the point of view of the control, this operation has two main consequences: since the In port is disconnected, the only the optical path to access the MRRs is by the Add port; the Out port is not optically accessible by the light injected at the Add port.

This situation poses a key challenge to the tuning and locking of the coupled MRR filter of the Tunable Optical Add Drop Multiplexer (TOADM), since the reference light to which the system has to be tuned is only available at the Add port. This way, to perform the locking of the resonances to a reference wavelength, the add signal must be present.

To circumvent this issue, we investigated the possibility to use optical power information at the Drop port of the filter for the tuning and locking. The results shown in the next section demonstrate that a very good convergence can be achieved by using the procedure described in Algorithm 1. The functional

diagram of the filtering unit is shown in Fig. 7a, where the CLIPP is shown at the Drop port, and a microphotograph of the fabricated device is shown in Fig. 7b. A detail of the filtering structure *per se* is shown in Fig. 7c, where also the thermal isolation deep trenches are visible in the middle of the rings and on top of the switching arm of the unbalanced MZ used as tunable coupler.

The switch off (Step 2) and switch on (Step 4) are the operation of the MZ tunable coupler as discussed in Sec. II-B. The use of a Look Up Table (LUT) (Step 3) to make a coarse selection of the channel enables a fast and rough tuning, that will bring the resonances close to the desired channel. However, due to thermal crosstalk from other devices on the chip, it is expected that this tuning will not place the filter in the exact position, providing sub-optimal spectral responses. In the following, some more details on the overall implementation of the algorithm is provided.

Algorithm 1 Hitless tuning of third order filter

1: **procedure** TUNE TO NEW CHANNEL
2:     Disconnect filter from bus and add/drop using MZIs
3:     Coarse tune of the three rings using LUT
4:     Connect filter to bus and add/drop using MZIs
5:     Enable continuous automatic tuning

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1) Step 1. Request to tune to new channel: The procedure is started whenever a channel reconfiguration is requested. Such request might come, e.g., from a network planning algorithm or simply by the manual request from the network operation.

2) Step 2. Filter disconnection: On this step, the filter is disconnected from the main bus, so that the MRRs resonances can be tuned with no impact on other channels. Looking at the filter from the Add port it behaves as an all-pass filter consisting of 3 MRRs coupled to a single bus waveguide.

3) Step 3. Coarse tune with LUT: Using pre-evaluated heater voltage points for each channel, heaters are assigned to the desired points. This process enables time saving for channel selection, but it comes with some residual tuning errors, mainly due to thermal crosstalk effect between the MRRs of the filter.

4) Step 4. Filter connection to the bus waveguide: Although the filter after coarse tuning exhibits a spread of the MRR resonances, in this condition the MZI tunable coupler can be switched on to connect the filter to the bus line without significant effects on the neighbor channels.

5) Step 5. Continuous automatic tuning: Once the coarsely tuned filter is connected to the bus waveguide, the add-to-drop in-band isolation increases. In this condition, the amount of optical power in the monitor should be enough to be used to lock the filter to the desired wavelength, using an appropriated continuous control algorithm. In our case, the TED technique [11] was used.

The algorithm for tuning and locking of the filter exploits advantageously the input signal at the Add port of the filter and the information provided by the monitor at the Drop port of the filter. After Step 4, the filter is connected back to the bus waveguide and the signal dropped from the In-to-Out waveguide arrives at the drop monitor together with the

Add signal, since both are at the same wavelength. Thus, the monitor must be able to discriminate the Add signal from other signals that could arrive simultaneously at the monitor, even if they are at the same wavelength.

To measure the power of the Add signal, regardless of the presence of the dropped signal, the channel labeling technique presented in section II-D and with more details in [17] and [19], is used. The Add signal label is inserted by a thermally driven MZI at the Add port as shown in Fig. 7b. Label frequencies in the range of a few kHz will be used and channel discrimination will be achieved by simply demodulating the monitor output signal to the frequency of the applied dithering.

IV. CHARACTERIZATION AND OPERATION

A. Filter response

Since fabrication tolerances are very strict for such high performance filters, the performance of the filter as fabricated is far from design target. It can be seen in Fig. 9 that the as fabricated response (blue curves) is far away from the target, and the three resonances of the filter are not aligned. Another issue is seen when the LUT values are applied to the filter. The green and red curves are the values that come from the LUT for two different target channels. Again, it can be seen that the filter profile is not inline with the specifications values. This is due to thermal crosstalk from other components on the chip that heat up the system and drift the spectral response of the filtering element. Only after applying the automatic control loop the filter performance is achieved as shown in Fig. 10.

Fig. 11 reports the convergence of the automatic tuning algorithm for different initial conditions of the filter. The algorithm makes use of the TED technique [11] to tune and lock the MRRs. With this technique, the thermal phase controller of all the MRRs are tuned simultaneously at each iteration of the algorithm to minimize the target error function, which in this case is the label power at the CLIPP. The power monitored by the CLIPP at the Drop port is shown, the absolute values being equal to the coupled power to the Add port decreased by the filter isolation and the pilot tone modulation depth. Note that only a small portion of Ch. 1_{Add} arrives at the Drop port, about $20\,\mathrm{dB}$ below the input power, corresponding to the isolation of the filter. For every tested starting condition the filter locking converge in few tens of iteration, each one corresponding to around 0.1 seconds.

Due to the wavelength dependence of the couplers, the performance of the filter in L and C bands is not the same, nonetheless similar results are also achieved and the full process is shown in Fig. 10 for the L band.

B. Hitless operation

To evaluate the effectiveness of the hitless tuning, the Bit Error Rate (BER) of Ch. 0 (Fig. 7a) was monitored during the tuning procedure. Fig. 12 shows the BER measurements of a channel transmitted from the input to the output port of the filter for case of hitless and non-hitless reconfiguration. The horizontal axis shows the instants in which a measurement of the BER was done. The BER form the 10 Gbps channel was measured with intervals of $300\,\mathrm{ms}$. When the filter is
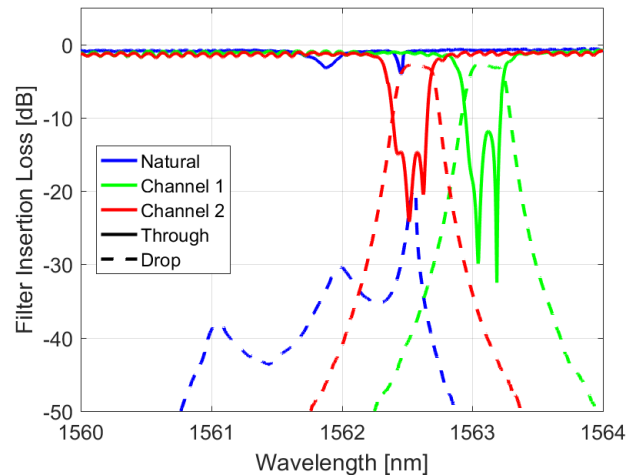

Fig. 9. Tuning of the filter for two different channels and its natural response.
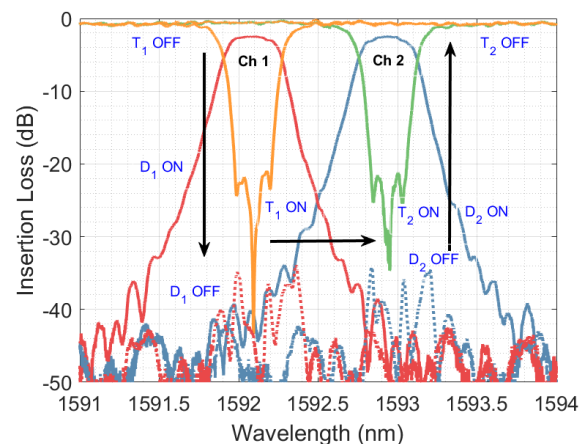

Fig. 10. Spectral response of the hitless filter during reconfiguration steps.

disconnected from the bus (solid blue line), the BER remains almost unchanged during the tuning of the filter, demonstrating that hitless tuning can be performed. In contrast, if the tuning is performed when the filter is connected (dashed red line), strong BER degradation is observed when the filter wavelength crosses the carrier wavelength of Ch. 0.

C. Multiple channel automatic tuning

The described locking technique can be used to automatically generate a LUT for channels in any specific grid. By applying the technique to four different channels spaced at $50\,\mathrm{GHz}$, we obtained the results shown in Fig. 13. It can be seen that very good filter shape is obtained for all the tested filters an channels. As mentioned previously, the smaller isolation on the C-Band is due to the wavelength dependence of the couplers, that in the C-Band present a smaller coupling coefficient. Still on Fig. 13 one can also note an excess loss of about $20\,\mathrm{dB}$. Such additional loss comes from the coupling to the chip. Our design uses grating couplers, which in this wavelength region have an insertion loss of about 9 dB per grating. The excess loss from the glass transposer by itself
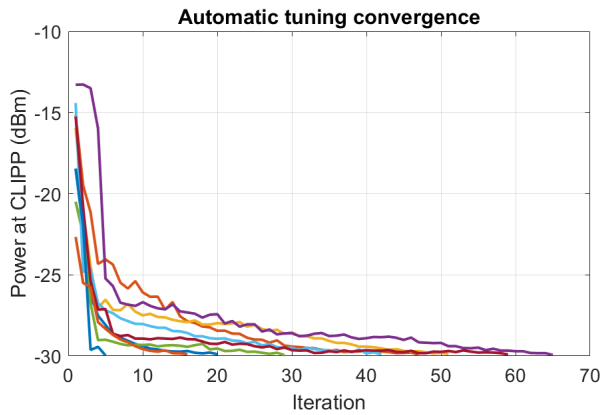
Fig. 11. Convergence of the tuning algorithm for diverse initial conditions. The diverse curves are for cases in which the system was being reconfigured for different channels on the channel grid.
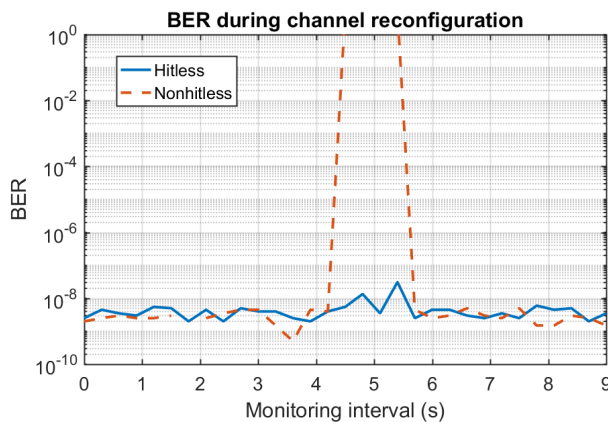

Fig. 12. BER measurements of the already established channel CH. 0 (1592.5 nm) during reconfiguration of the filter from Ch. 1 (1592.1 nm) to Ch. 2 (1592.9 nm) with hitless reconfiguration (blue curve) and nonhitless reconfiguration (red dashed curve)

is below $1\,\mathrm{dB}$ and the remaining $2\,\mathrm{dB}$ are from propagation losses, since the bus waveguide on this chip design is about $1\,\mathrm{cm}$ long.

V. CONCLUSION

In this work a comprehensive design, analysis and test of the key wavelength processing unities and test structures were done. To undergo this duty, several building blocks are available in commercial SiP foundries, but the fabrication tolerances of each one poses challenges on the calibration and operation procedures.

The control of SiP technology is still a limiting factor to its mass adoption. We proposed a strategy that can be used to control complex optical circuits to be used not only in telecommunication applications but also in many other industries that might profit from the integration capabilities offered by SiP. At the hearth of the strategy lies the use of channel labels used to individuate optical signals that are possibly mixed not only among other channels but even amid optical noise. By using this strategy, we were able to calibrate and operate a third order MRR designed and fabricated in SiP.
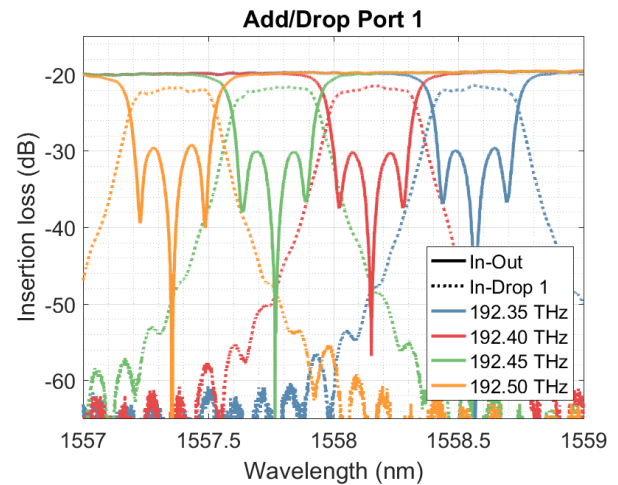

Fig. 13. Spectral responses after automatic tuning for four different channels.

On of the most critical aspects that was observed in the design was the wavelength dependence of the directional couplers used in this work. In MRR the optical bandwidth of the filters is determined by such couplers, thus the overall performance of the filter along the operation bandwidth is directly related to this variation, which cannot be made arbitrarily small in for small coupling coefficients.

Finally, a complete functional device to operate hitlessly in an optical network was demonstrated, including the demonstration of the insensitivity of the neighbor channel to the reconfiguration of the filter. The demonstration made use of transparent devices, but standard photodiodes can also be used to the same goal, enabling currently deployed systems to take profit from such technique.

APPENDIX

PHOTONIC BUILDING BLOCKS

A. Directional couplers

To achieve the required coupling coefficient in small rings, the use of bent directional couplers is proposed [20]. In such device the coupling region is formed by the ring resonator and a bent waveguide, whose bent is in the same direction of the ring. The transition regions are bents in the opposite direction of the ring. With this geometry higher power coupling values are achieved in a still small footprint. A design consideration that must be taken is that the product between each radius and effective indexes,

$$R_1 n_{eff,1} = R_2 n_{eff,2}, \tag{2}$$

must be equal. This is to guarantee phase matching between both waveguides, since the coupling region is bent.

Numerical simulations were held at a wavelength of $1550\,\mathrm{nm}$ to obtain the theoretical coupling coefficient as a function of the coupling angle of the device. In the simulations, an external radius of $12.11\,\mathrm{\mu m}$ and internal radius of $11.45\,\mathrm{\mu m}$ were used. A gap of $200\,\mathrm{nm}$ between the waveguides was considered and waveguide widths of $490\,\mathrm{nm}$ and $430\,\mathrm{nm}$ were respectively used for the internal and external waveguides.

Standard Silicon On Insulator (SOI) waveguide thickness of $220\,nm$ were used, and as refractive indexes at $1550\,nm$ for Silicon and Silica 3.4799 and 1.4505 were respectively used.

With the theoretical values in hands, one is able to design an optical filter and choose the proper coupling coefficient required for the targeted filter shape. For the bent couplers, the simulated relation between coupling angle and power coupling coefficient is almost linear and for $k_4 = 0.233$ the obtained coupling angle was $23°$ and for $k_a = k_b = 0.062$ the required angle was $7.0°$. For the inner couplers that need to be done with bents with opposing radius, the gap required for $k_2 = k_3 = 0.009$ was $230\,nm$.
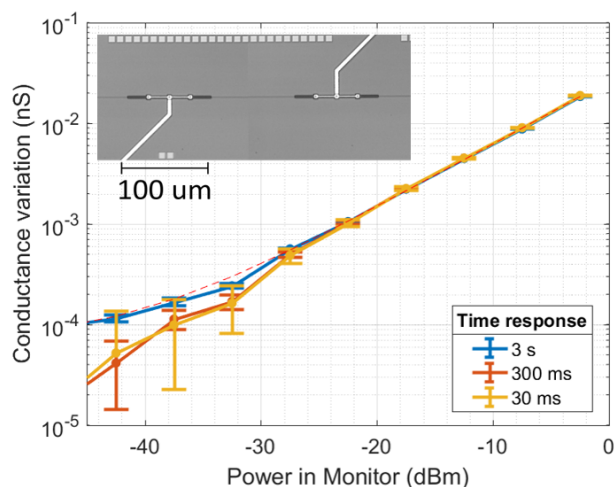
B. Transparent channel monitoring

Fig. 14. Measured CLIPP performance vs. optical power. In the inser a micro-photograph of a CLIPP realized on a SiP commercial platform

The CLIPP monitors the light intensity in waveguides by measuring the change in the resistance of the core segment between two metal pads. A photo of a CLIPP realized by a commercial foundry is shown in the inset of Fig.14 where the two pads are realized in Titanium Nitride (TiN). The change in waveguide resistance versus optical intensity has a nonlinear dependence, almost linear on a loglog scale. For mW range optical power in the waveguide, the conductance change ΔG_{wg} is typically in the nano Siemens scale. A typical response of the CLIPP device for silicon photonics is shown in Fig. 14.

C. Phase actuators

To maximize simultaneously the CLIPP and heater performance one can use the same layer for both devices and place this layer at $1\,\mu m$ of the waveguide layer. This distance allows for good heater efficiency without much optical loss, and also allows the CLIPP device to work with a higher access capacitance. In addition, to optimize even further the heater efficiency, deep trenches were used since they aid the heating of the waveguide by confining the thermal field around them. To this aim, deep trenches were placed both inside and around the ring resonators.

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