Design of a 16 x 16 fast-gated SPAD imager with 16 integrated shared picosecond TDCs for non-line-of-sight imaging

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ABSTRACT

We present the design of a new fast-gated 16 x 16 silicon SPAD array developed in a 0.16 μm BCD technology with built-in 6 ps resolution TDCs (Time-to-Digital Converters), optimized for Non-Line-Of-Sight imaging. The high temporal resolution is achieved by sharing one high-performance TDC among 16 SPADs, without losing spatial resolution, thanks to an identification logic capable of detecting and rejecting collisions. In the SPAD frontend, a low-threshold comparator minimizes temporal jitter, while an active quenching circuit reduces afterpulsing. An event-driven readout scheme optimizes data transfers, however a standard frame-driven photon-counting only mode is also available. The goal is to enable quasi real-time NLOS scene reconstruction by parallelizing the acquisition across multiple spots. Thanks to its high temporal resolution, the detector can be exploited also in other scientific applications, such as clinical diagnostic (with Time-Domain Near Infrared Spectroscopy) and LiDAR (Light Detection and Ranging).

Keywords: Non-Line-Of-Sight imaging, Fast-gated SPAD, SPAD imager, Integrated TDCs, Photon counting, Time-resolved imaging, Geiger-mode APD, SPAD array

1. INTRODUCTION

Non-Line-Of-Sight (NLOS) imaging aims at identifying and tracking objects outside of the direct field-of-view of the observer, typically hidden behind a wall around a corner. The capability of reconstructing NLOS scenes has been demonstrated by using radio waves [1], acoustic waves [2] and light [3].

Out of the multiple techniques that have been shown to be capable of reconstructing NLOS scenes, the most promising one is based on using pulsed LASER sources and time-resolved detectors: a short LASER pulse is shone onto a surface that is directly exposed both to the observer and to the NLOS scene as shown in Fig. 1; the LASER light will then scatter off the surface, generating a spherical wave that will interact with the NLOS scene; the objects in the scene will back-scatter some of the photons onto the relay wall that is imaged with a time-resolved detector, collecting the arrival time of the photons. A 2-axis galvanometer mirror allows an X-Y scanning and a back-projection algorithm can be used to reconstruct the NLOS scene based on the information retrieved [4].

The main problem of this technique is that the back-scattered signal, coming from multiple bounces, suffers a high attenuation, resulting in a very faint light signal, thus requiring single-photon sensitivity. Moreover, such signal is preceded by a very strong pulse, corresponding to the spherical wave originated by the first light bounce directly hitting and potentially blinding the detector to the true NLOS signal. As such, it is of utmost importance the use of a time-gated detector, that can be disabled during the arrival of the first bounce and activated only when the NLOS signal is expected.

The field of non-line-of-sight sensing has seen a growing interest for its potential applications in monitoring hazardous environments, search and rescue, remote sensing and, potentially, in autonomous vehicles. Furthermore, a growing interest for NLOS imaging has been expressed for space exploration, with the ability for an orbiting satellite to map not only the visible surface but also inside caves and craters whose interior is not usually visible.

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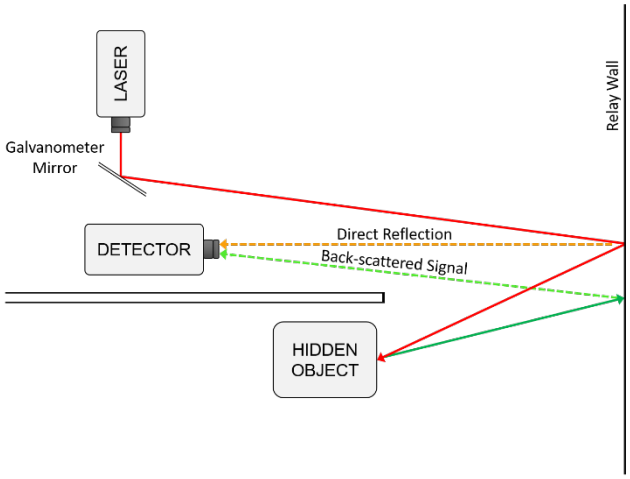

Fig. 1. Schematic representation of a Non-Line-Of-Sight setup.

2. SPAD ARRAY ARCHITECTURE

2.1 NLOS requirements

Imaging systems for NLOS scene reconstruction require:

- Fast-gated SPADs, to effectively perform time-filtering of incoming photons
- High detection efficiency
- Low temporal jitter (ideally < 50 ps FWHM)

The goal of developing the imager we present is to combine all the above requirements while at the same time allowing parallelized measurements in order to reduce the overall acquisition time.

Single pixel detectors with all the aforementioned prerequisites for high-resolution NLOS reconstruction exist [3], but no multi-pixel imager is available. The single-pixel solution is a fast-gated SPAD requiring the use of external TCSPC boards. As such, parallelization is theoretically possible, but impractical, as it would be limited by the number of channels available in the TCSPC instrumentation and would lead to a bulky and expensive system.

On the other hand, many time-gated SPAD imagers have been presented in the literature, but they either lack the temporal resolution required [5], or do not have an effective SPAD gating mechanism to reject unwanted photons [6]-[7], or even only operate in photon-counting mode, relying on gate-shifting to gain their temporal resolution [8]-[9]. This last solution is unable to provide any gain in NLOS scene acquisition speed, as the increase in number of pixels would be counteracted by the requirement of shifting the gate thousands of times to reconstruct the arrival times of photons with high resolution over tens of nanoseconds of range, required for reconstruction of room-sized scenes.

2.2 BCD technology

We chose to design the detector in a 0.16 µm BCD (Bipolar-CMOS-DMOS) technology for the ability of integrating SPADs with state-of-the-art detection performance and the availability of thick and thin oxide transistors to optimize the imager performance. SPADs in this BCD technology have been shown to obtain significantly higher Photon Detection Efficiency (Fig. 2) with respect to typical CMOS SPADs [10], while still keeping the noise low [11]. Furthermore, they present low timing jitter and a very fast exponential tail in their temporal response, making them perfectly suited for NLOS imaging with sharp time filtering.

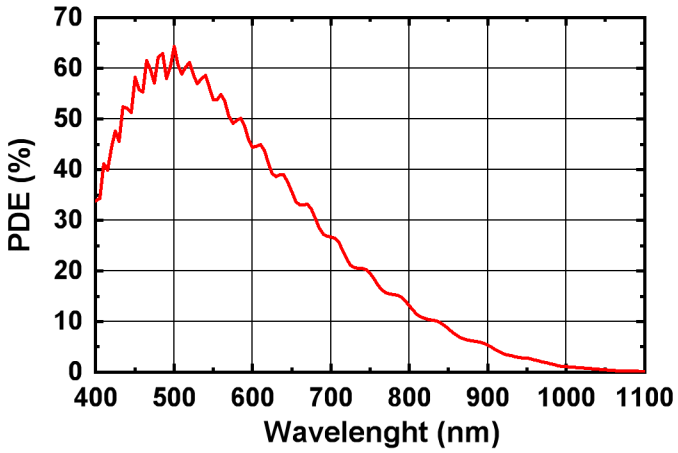

Fig. 2. Photon Detection Efficiency measured for a square BCD SPAD with 32 µm side and rounded corners when operated at 5 V of excess bias.

This technology provides also triple-well isolation with deep trenches, allowing us to isolate the gating circuit from the highly sensitive analog circuitry, while still achieving monolithic integration. The power handling capabilities allowed us to place decoupling capacitors for all voltage rails on-chip, including the cathode voltage supply (~ 30 V) to minimize voltage fluctuations that might impair gating performance.

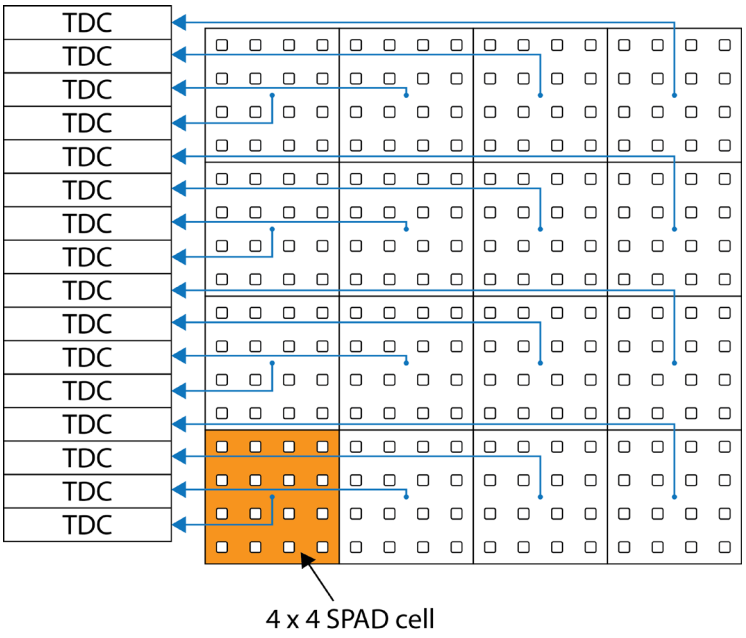

Fig. 3. Simplified representation of the array architecture, showing the division in cells sharing a single TDC, and the off-pixel electronics placed on one side of the sensor array.

3. IMAGER ARCHITECTURE

The imager features 16 x 16 pixels, where each pixel is composed of a square SPAD with rounded corners and 32 µm sides, placed at a pitch of 100 µm, yielding a fill-factor of 9.6 %. The SPAD distribution matches the one of a previous array we developed [5] to ease the future integration of microlenses. The SPADs are operated at a maximum excess bias voltage of 5 V in order to obtain optimal temporal response and detection efficiency, while still having low noise.

SPADs are grouped in cells, each composed of 4 x 4 pixels. Each cell shares a single high-performance TDC placed in the chip periphery, as shown in Fig. 3. The chip layout has been optimized to allow for easy scaling by tiling multiple 16 x 16 blocks, since the timing electronics is placed on one side of the array only.

Each TDC has a dedicated pair of serial output pads in order to implement an event-driven readout method, thus optimizing data transfers towards an FPGA. The maximum conversion rate for each TDC is more than 10 M events per second, for a maximum overall throughput of ~ 6 Gbps.

3.1 Pixel structure

The SPAD frontend (Fig. 4) is designed to allow operating the SPAD at a maximum of 5 V excess bias, by employing thick oxide transistors. The 5 V logic is enclosed in its own isolation well, and has a separated power supply and ground lines, to avoid injecting disturbances in the low voltage logic region.

M4 and M5 transistors are controlled with the GATE signal (0 ÷ 5 V) and are used to activate the SPAD by bringing its anode to ground and to disable the SPAD by raising its anode voltage to 5 V. M1 and M2 transistors normally operate in ohmic region and are used both to choose the gate opening edge duration (transition time changes by enabling one or the other or both) and to quench the SPAD after the avalanche is detected by turning them off. M3 transistor is used as a cascode to safely connect the SPAD anode to a low-voltage comparator.

The comparator (Fig. 5) uses a PMOS input stage and is used to minimize the sensing threshold and reject the gating disturbance. In order to maximize speed, the comparator is implemented with thin oxide transistors, and as such can only tolerate a maximum input voltage of 1.8 V, thus requiring the use of the cascode thick oxide transistor.

The comparator uses a simple structure with positive feedback to speed up transitions. The input pair (M4-M5) is purposely mismatched in order to introduce an unbalance, which leads to an input offset that is used to set the switching threshold. Such threshold is about 25 mV (nominal), aiming to minimize the jitter contribution due to the statistical buildup of the avalanche in the SPAD. This should allow to obtain a timing jitter close to the one reported in [11]. More control on the threshold is made possible by the addition of M4' transistor, which can be in parallel to M4.

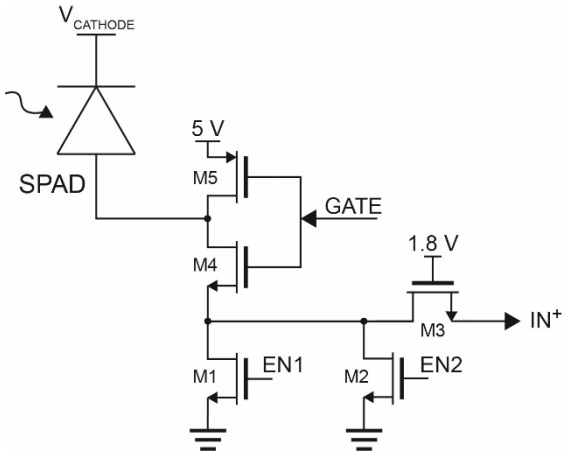

Fig. 4. Schematic of the SPAD frontend circuit. M1 and M2 are used to sense the avalanche current and control the activation edge speed, M3 protects the comparator from overvoltage events and M4-M5 perform the gating operation.

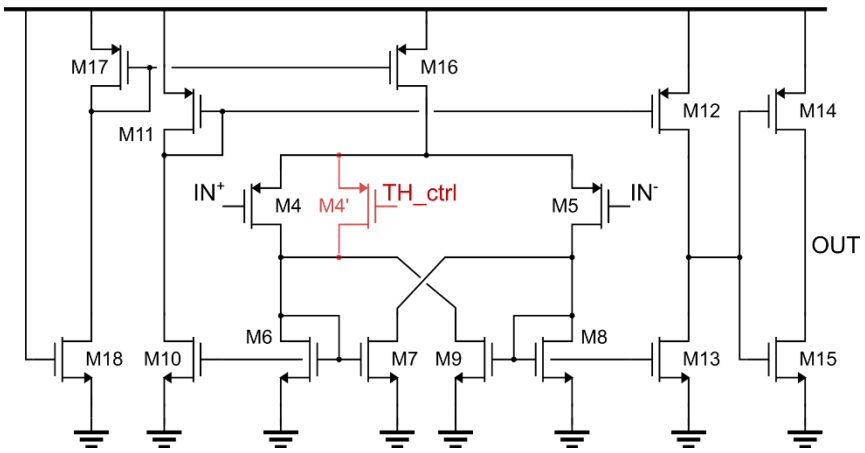

Fig. 5. Schematic of the comparator. M17-M18 bias the stage, while the cross-latch formed by M7-M9 provides positive feedback to speed up transitions. The input stage M4-M5 is purposely unbalanced to introduce a deterministic offset.

3.2 Identification Logic

Each cell includes a circuit that identifies the firing SPAD, providing a 4-bit binary output with the coordinates of the SPAD inside the 4 x 4 array and an additional validation output. The logic is able to identify if a collision happened (e.g. two or more SPADs fire almost simultaneously within the same cell) and, in case of such event, given the possibilities of misassignment of the coordinates and timing distortion, the output is invalidated and the TDC conversion aborted. This allows to quickly reset the cell to a state where it can detect a new event, minimizing dead time.

3.3 Time-to-Digital Converters

Each of the 16 TDCs is based on two interpolators, one for the START signal (corresponding to the photon detection) and one for the STOP signal (synchronous with the LASER pulse), to implement the sliding scale technique and improve linearity, as shown in Fig. 6a. The TDC is based on a multistage interpolation architecture [12].

The TDC makes use of a 10-bit counter with 420 MHz reference clock (T_{ck} = 2.4 ns), thus obtaining an FSR of about 2.45 µs. Two 10-bit interpolators are based on two interpolation stages each, as shown in Fig. 6b. The first stage uses the input signal to sample 16 phases of the reference clock and provides the coarse temporal information. The second stage uses a cyclic single-stage Vernier delay line to obtain a final resolution of about 6 ps.

To guarantee stability with respect to Process, Voltage and Temperature (PVT) variations, a coarse Delay-Locked Loop (DLL) is used to generate the 16-phase clock, while a dual fine interpolator bias circuit, composed by two other DLLs, is used to properly bias the fine interpolators to set the correct propagation delays and define the resolution of the converter.

The imager receives a global STOP signal, synchronous with the excitation laser, and its arrival time with respect to the reference clock is measured by the STOP interpolator and stored in an output register. The START interpolator measures the time interval between the START signal, synchronous to a photon detection, and the reference clock. The counter is placed in the START interpolator and it measures the number of clock periods between START and STOP signal ($T_{counter}$). For each interpolator, the coarse interpolation measures the delay (T_{c_START} and T_{c_STOP}) between the first clock phase after the rising edge of the input signal and the successive reference clock rising edge. The time delay between the input and the successive clock phase (T_{f_START} and T_{f_STOP}) is measured by the fine interpolator as the difference between HIT SYNC and CK SYNC pulses, through a coarse-fine synchronizer. The final START-STOP delay (T_{meas}) can simply be calculated by summing the times measured by the counter and the START interpolator minus the delay measured by the STOP interpolator (1):

$$T_{meas} = T_{counter} + \left(T_{c\_START} + T_{f\_START}\right) - \left(T_{c\_STOP} + T_{f\_STOP}\right) \quad (1)$$

The coarse interpolator is obtained with a DLL-based multiphase clock interpolation. The DLL uses a voltage-controlled delay line (VCDL), composed of 16 voltage-controlled delay cells (VCDC), through which the 420 MHz reference clock propagates. The total delay of delay line is locked to the reference clock thanks to a phase detector and a charge pump that sets the control voltage accordingly. The outputs of the 16 delay cells are tapped off to obtain a multiphase clock where every phase is ideally delayed from the previous one by a constant value equal to Tck / 16 = 150 ps stabilized against PVT variations. The state of the multiphase clocks is sampled by an arbiter circuit in correspondence of the rising edge of the input signal of the interpolator; this thermometric value is then converted into a binary value and stored in a 4-bit output register.

To obtain a resolution better than the intrinsic propagation delay achievable in this technology node, we implement a modified single-stage Vernier delay line, whose resolution is defined by the difference between the propagation delay of two cells, as shown in Fig. 7. This architecture is based on two delay loops in which HIT SYNC and CK SYNC pulses cycle through. The propagation delay of the cell in each loop is defined by a DLL and is such that the propagation delay of the cell in the HIT SYNC loop is longer than the propagation delay of the cell in the CK SYNC loop. At every cycle, the delay between CK SYNC and HIT SYNC reduces, and the cycling stops as soon as CK SYNC overcomes HIT SYNC.

The result of the conversion is given by the number of cycles needed to reach the termination condition and it is obtained with a 6-bit counter. Moreover, since the loops are based on single cells, the statistical mismatch between the two loops does not result in non-linearity, but just in gain error, which can be easily taken into account in post-processing.

The output of each TDC consists of the time-tag, the SPAD identifier and a validation bit to ensure that the conversion result is correctly associated to the originating pixel. After the EOC is asserted, the output data are loaded into a pair of shift-registers, and a FLAG signal is sent to the control FPGA to initiate the serial transfer automatically. During the serial transfer the TDC is ready to convert a new event, thus minimizing the dead-time between successive conversions.

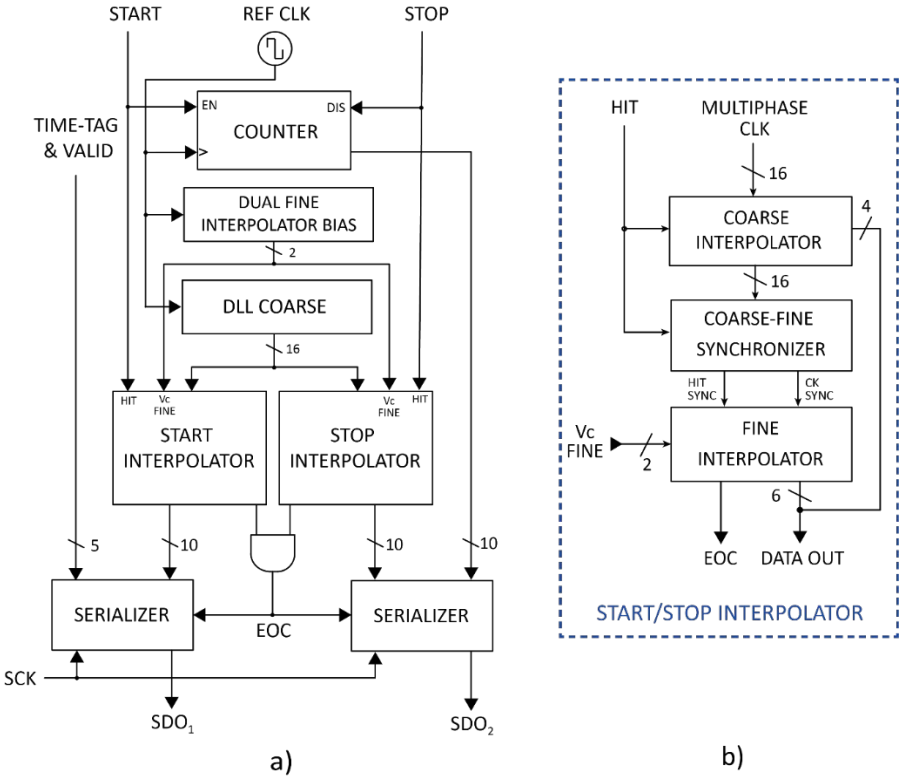

Fig. 6. Block scheme of the integrated TDC (a) and the START/STOP interpolator (b). The TDC is based on multistage interpolation to obtain picosecond resolution and long FSR. The serializer transfers the output data of TDC through two output pads.

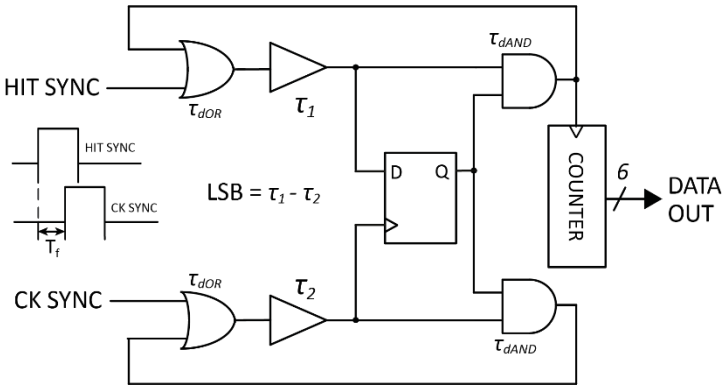

Fig. 7. Simplified schematic of the cyclic single-stage Vernier delay line implemented in the fine interpolator, whose resolution is defined by the difference between two delay cells.

4. CONCLUSIONS

We presented the design of a fast-gated SPAD imager with 16 x 16 pixels targeted for Non-Line-Of-Sight 3D imaging, combining the fast-gated performance previously only demonstrated for single pixels, with integrated high-resolution Time-to-Digital Converters. This new detector aims at enabling faster (video rate) acquisition of NLOS scenes by future integration in a fast-gated camera with high temporal resolution.

This imager (whose layout is shown in Fig. 8) can also find use in other scientific applications where high detection efficiency and low timing jitter are required, such as Time-Domain Near Infrared Spectroscopy (TD-NIRS) and LiDAR (Light Detection and Ranging).

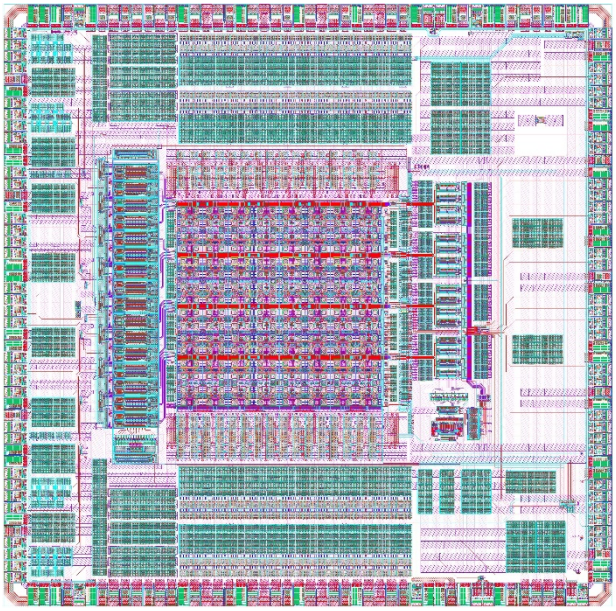

Fig. 8. Complete layout of the 16 x 16 SPAD imager with fast-gating capability. The die size is 4.8 × 4.8 mm^2

5. ACKNOWLEDGMENTS

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