Sub-nanosecond gating of InGaAs/InP SPAD

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ABSTRACT

Time gating for SPADs is exploited either for increasing their maximum count rate or for detecting faint signals hidden by strong unwanted light pulses. Here we describe two short-gate techniques for high-speed photon counting with InGaAs/InP SPADs: i) a sinusoidal gating system at about 1.3 GHz, with very low afterpulsing and high count rate; ii) a SiGe integrated circuit for sub-nanosecond gating with < 200 ps rising/falling edges.

Keywords: SPAD, photon counting, InGaAs/InP, gated mode, fast gating, sinusoidal gating, avalanche photodiode

1. INTRODUCTION

Time gating is becoming an important technique for Single-Photon Avalanche Diodes (SPADs), both for improving their performance (e.g. the maximum count rate) and for detecting faint signals hidden by strong unwanted light pulses.

A growing number of applications in the 1 μm - 1.7 μm wavelength range require single-photon detectors with high count rates (greater than a few Mcount/s), high detection efficiency (> 30%), low noise (few kcount/s), narrow temporal response (FWHM < 100 ps). InGaAs/InP SPADs show good performance and are suitable for practical and reliable systems, but their main drawback is the strong afterpulsing, which limits the maximum count rate [1]. Afterpulsing can be mitigated either by increasing the hold-off time (even > 10 μs), though strongly limiting the maximum count rate, or by reducing the avalanche charge (i.e. the current flowing through the device after photon detections). The latter approach is effective, but requires smart circuital solutions for working with short gates (<< 1 ns width) that quench the avalanche during its build-up [2]. Here we describe two short-gate techniques for high-speed photon counting with InGaAs/InP SPADs: i) a sinusoidal gating system at about 1.3 GHz, with very low afterpulsing (~ 1.5 %), high count rate (650 Mcount/s), high photon detection efficiency (> 30 % at 1550 nm), low dark count rate ($2.2 \cdot 10^{-5}$ per gate) and low timing jitter (< 70 ps FWHM); ii) a custom-designed SiGe integrated circuit (ASIC) for sub-nanosecond gating with < 200 ps rising/falling edges and low (< 30 ps FWHM) time jitter.

2. SINUSOIDAL GATING OF INGAAS/INP SPAD

Short gating techniques exploit sub-ns gate pulses to quench the avalanche during its build-up, thus abruptly reducing the number of charge carriers that can be trapped. However, owing to the capacitive feed-through of gate pulses, the signal at the readout node includes a small avalanche signal (whose amplitude is just few millivolts) and a strong residual fraction of the sinusoidal gating voltage, having an amplitude orders of magnitude higher than the avalanche pulse itself). Various solutions have been reported in literature to mitigate this effect, including: i) self-differencing circuits [2][3], which require fine-tuned delays; ii) notch filters at the gate frequency and its harmonics [4]. However, hardware changes either on self-differencing delays or notch filters are needed to adjust the gate frequency (e.g. when changing the frequency of the photon source). Conversely, broadband circuit solutions such as iii) the harmonic subtraction technique [5] and iv) the balanced detector configuration [6], which actively synthesize a signal that cancels the gate feedthrough, permit to adjust the gate frequency in a wide range and synchronize it to any external photon source.

In the balanced detector configuration (see Figure 1), the InGaAs/InP SPAD is paired with a "dummy" structure, i.e. a diode that mimics the electrical response of the detector, but it is insensitive to photons. Both diodes are reverse biased at the SPAD breakdown voltage, while two opposite sinusoids are AC coupled to their anodes. The SPAD is periodically

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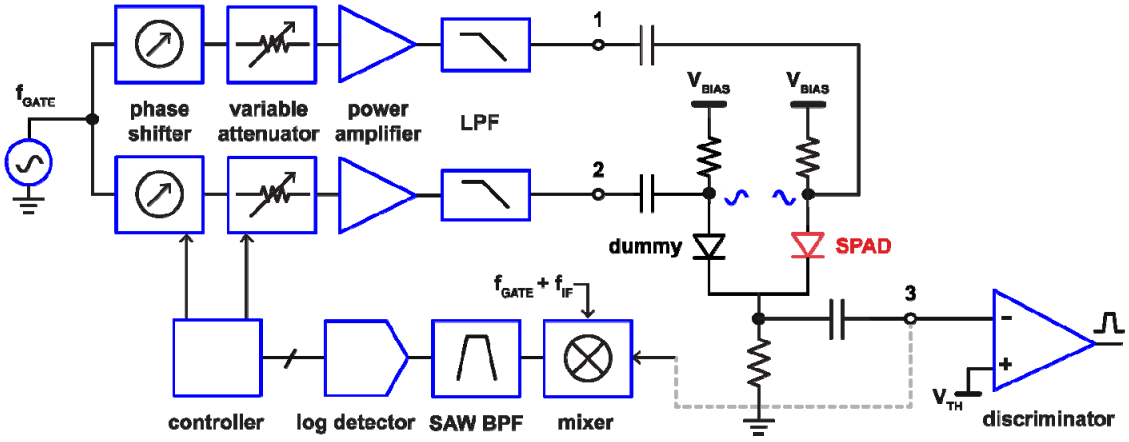

Figure 1. Simplified block diagram of the sinusoidal gated SPAD-dummy balanced configuration for cancelling the capacitive coupling of the gate at the discriminator input. LPF = low pass filter, SAW BPF = surface acoustic wave band pass filter.

biased above its breakdown voltage by the gate signal, while the "dummy" is always under its breakdown voltage. The SPAD gate feed-through is balanced with its own anti-phase copy (propagating through the "dummy" path) at the common cathode node.

The system here described has been characterized with a 25 μm active area diameter InGaAs/InP SPAD [1]. In order to maximize the matching between the SPAD and dummy electrical responses, both diodes are in the same chip. The "dummy" is another p-n junction with breakdown voltage about 10 V higher than that of the SPAD. The SPAD-dummy chip is mounted on a three-stage thermoelectric cooler and packaged in a TO-8 package. At about 1.3 GHz, the forward transmission coefficient through the devices inside the package is about -10 dB. Despite the high degree of symmetry between the SPAD and dummy paths, component tolerances and temperature drifts may introduce residual mismatches. Therefore, the relative amplitude and phase of the two sinusoids need to be finely and continuously adjusted for achieving a good cancellation of the feedthrough signal at the cathodes. In detail, it can be estimated that the phase has to be controlled with a resolution of 2 mrad and the amplitude with a resolution of 0.2%, in order to achieve a suppression of the feedthrough of about 50 dB (resulting in a residual feedthrough power lower than 35 dBm, for a SPAD excess-bias voltage of 5 V) . To this aim, we introduced a feedback control loop that starts minimizing the gate feed-through power by adjusting the relative amplitude and phase of the two sinusoids with progressively smaller step sizes. Once the gate feedthrough has been reduced below the desired avalanche discrimination threshold, the feedback loop keeps monitoring and adjusting the relative amplitude and phase shift to compensate for temperature drifts.

Figure 2 shows a voltage waveform acquired at the discriminator input. Thanks to the very low noise level (below few mVpp), avalanche events are distinguishable from the noise floor. However, the amplitude of the avalanche signals varies widely from one avalanche event to another, because the excess bias is not constant within the gate. Therefore, a low discrimination threshold is needed for preserving low-jitter temporal response of the detector.

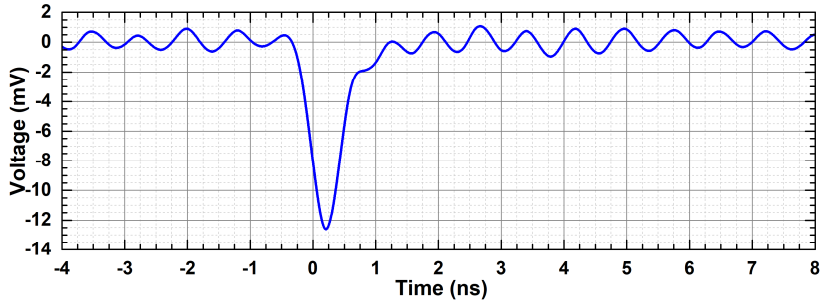

Figure 2. Output signal after gate feed-through cancellation: the pulse is the response to a single photon (avalanche).

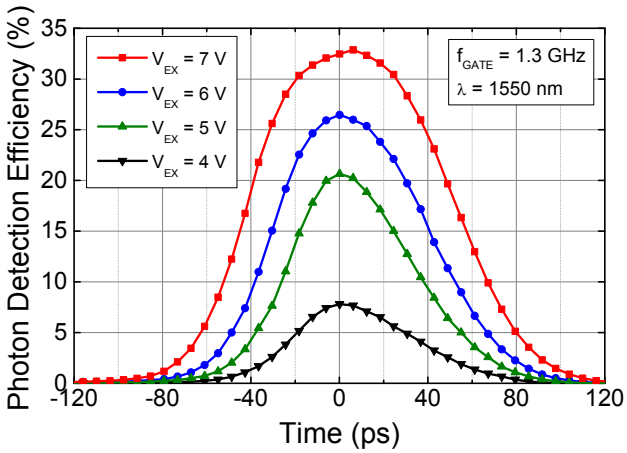

Figure 3. Photon detection efficiency of PoliMi InGaAs/InP SPAD at $\lambda = 1550$ nm, within a sub-ns gate window.

This system demonstrated high performance: very low afterpulsing (~ 1.5 %), high count rate (650 Mcount/s), high photon detection efficiency (> 30 % at 1550 nm, see Figure 3), low dark count rate ($2.2 \cdot 10^{-5}$ per gate) and low timing jitter (< 70 ps FWHM).

3. SIGE INTEGRATED CIRCUIT FOR SUB-NANOSECOND GATING

The miniaturization of the front-end circuitry is fundamental for the development of multi-pixels sensors, such as linear and two-dimensional arrays of InGaAs/InP SPADs, that nowadays are required by many applications. Of course, also single-pixel systems will benefit from this improvement, decreasing their size and reducing their power consumption. An integrated circuit, developed at Politecnico di Milano, is able to operate SPADs in gated mode and to read the avalanche pulses with low time jitter, even during the gate window rising edge [7]. It employs differential sensing in order to reject gate feed-through and achieve very short quenching time, while keeping a fast-rising edge of the gate. Therefore, photons arriving during the rising and falling edges are properly detected with low timing jitter. The circuit is built in a reliable 0.35 µm SiGe-CMOS technology, which also exploits fast SiGe bipolar transistors. The control logic of this integrated circuit is fully static (no lower limits in the gating frequency range), there is no limitation on the maximum duration of the gate window and the chip can also be employed in free-running mode. The integrated circuit has been fully-described in ref. [7].

The circuit has been mounted, together with the InGaAs/InP SPAD, inside a TO-8 package, onto a three-stage thermoelectric cooler able to reach a temperature of 230 K (see Figure 4). We also built an electronic system, made of three main boards (see Figure 5), for operating such system-in-package. The overall size of the system is 40 mm x 50 mm x 70 mm.

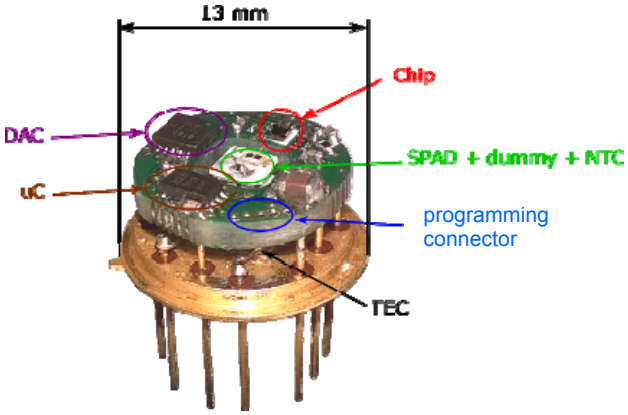

Figure 4. System-in-package including the InGaAs/InP SPAD, its sub-ns gating and quenching circuit, a compact microcontroller and other ancillary circuits. The detector is cooled with a three-stage TEC, also mounted inside the same package.

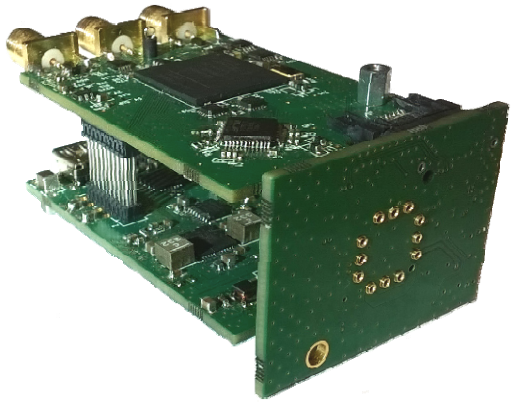

Figure 5. Printed circuit boards inside the photon-counting module developed around the system-in-package with the SiGe integrated circuit and the InGaAs/InP SPAD.

During the experimental characterization, we assessed that the rising edge is pretty fast (about 200 ps). Furthermore, very short gates can be generated: Figure 6 shows that gates with a full-width at half maximum of few hundreds of picoseconds can be obtained. The quenching time is below 1 ns and the system is able to achieve high gate repetition rates (up to 250 MHz). This approach still guarantees low timing jitter (FWHM < 90 ps). Finally, thanks to the fast avalanche quenching, we measured a reduction of the afterpulsing allowing to apply a hold-off reduced to at least a factor two compared to a discrete-components solution at the same afterpulsing probability (when gates longer than a few nanoseconds are applied), at the benefit of a higher maximum count rate.

4. CONCLUSIONS

This paper reports about two short-gate techniques for high-speed photon counting with InGaAs/InP SPADs.
In the first approach, a photon-counting system is based on InGaAs/InP SPADs gated by a high frequency sinusoid. The joint use of a balanced detector configuration (with SPAD and "dummy" integrated in the same chip) and proper fine-tuning of the relative amplitude and phase shift guarantee to achieve a good suppression of the gate signal feedthrough at the readout node, thus allowing for detecting avalanches with very low thresholds. Moreover, this configuration allows to adjust the gating frequency in a wide range, from 1 to 1.6 GHz, with the gate sinusoid that can be different from that of the photon source. Finally, a feedback control loop automatically optimizes the gate feed-through suppression in order to have a stable system that can operate continuously in real settings.

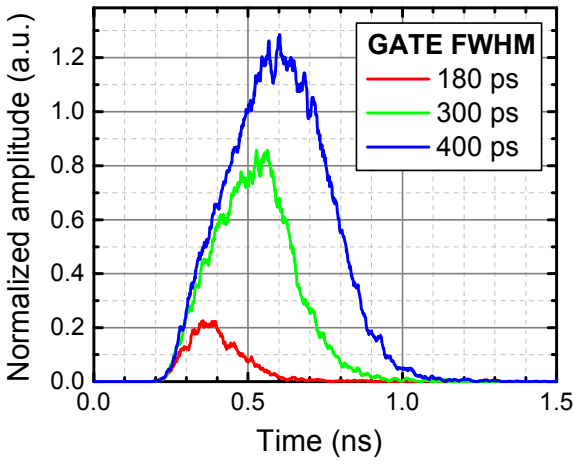

Figure 6. Short gate applied to an InGaAs/InP SPAD by the fast-gating ASIC: a width < 300 ps is feasible.

In the second approach, a SiGe integrated circuit is used for sub-nanosecond gating of InGaAs/InP SPADs with < 200 ps rising/falling edges. We also described the system where such circuit is exploited. The short quenching time keeps the needed hold-off time at least a factor of two shorter than discrete-components solution, at the same afterpulsing probability, when long (more than few nanoseconds) gates are applied.

ACKNOWLEDGEMENTS

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