Linear Multi-Step Discretization Methods with Variable Step-Size in Nonlinear Wave Digital Structures for Virtual Analog Modeling

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***Abstract*—There is a growing interest in Virtual Analog modeling algorithms for musical audio processing designed in the Wave Digital (WD) domain. Such algorithms typically employ a discretization strategy based on the trapezoidal rule with fixed sampling step, though this is not the only option. In fact, alternative discretization strategies (possibly with an adaptive sampling step) can be quite advantageous, particularly when dealing with nonlinear systems characterized by stiff equations. In this article, we propose a unified approach for modeling capacitors and inductors in the WD domain using generic linear multi-step discretization methods with variable time-step size, and provide generalized adaptation conditions. We also show that the proposed approach for implementing dynamic (energy-storing) elements in the WD domain is particularly suitable to be combined with a recently developed technique for efficiently solving a class of circuits with multiple one-port nonlinearities, called Scattering Iterative Method. Finally, as examples of application, we develop WD models for a Van Der Pol oscillator and a dynamic diode-based ring modulator, which use different discretization methods.**

***Index Terms*—Wave Digital Filters, Nonlinear Audio Circuits, Virtual Analog Modeling, Reactances**

I. Introduction

Wave Digital (WD) Filters [1], [2] have been extensively used in the audio signal processing community both for Virtual Analog modeling [3]–[9] and, combined with Digital Waveguides [10], [11], for Sound Synthesis through physical modeling [12]–[15]. WD structures have even been used for designing spatial filters in beamforming applications based on Differential Microphone Arrays [16]. It is only in the past few years, however, that Virtual Analog modeling has truly focused on the WD domain. Numerous articles, in fact, have recently appeared in the literature, proposing WD realizations of circuits containing linear and nonlinear elements such as operational amplifiers [6], [17], [18], nonlinear transformers [19], diodes [6], [20]–[23], vacuum tubes [24], [25] and transistors [26]–[30], which were not initially addressed in the original literature on WD Filters [1]. Dynamic circuits with up to one nonlinear element can be implemented using *explicit* (i.e. without delay-free loops) WD structures [2], [31]. This is a considerable advantage of WD modeling over Virtual Analog modeling methods [32]–[35] that work in the Kirchhoff domain (of voltages and currents), as they are typically characterized by sets of implicit equations and involve iterative solvers. This benefit, however, does not apply to circuits with multiple nonlinearities, as not all the delay-free loops can be removed [36], therefore we cannot avoid implicit equations. Even in these cases, however, working in the WD domain has proven beneficial. For instance, in [7] a method is introduced that allows to group all the nonlinear elements "at the root" of the WD structure, thus enabling the nonlinear part of the circuit to be separated from the linear one; then, the multi-dimensional nonlinear system of equations describing the nonlinear part is solved using the K-method with tabulation [27], [37] or multi-dimensional Newton-Raphson (NR) solvers [29]. Another iterative technique developed in [38] exploits the contractivity property of a class of WDFs for solving circuits with multiple nonlinearities making the wave signals circulate in the WD structure up to convergence. In [38] dynamic elements are accommodated introducing fictitious delays and employing the multi-dimensional WDF formalism. A different fixed-point method, known as Scattering Iterative Method (SIM), is introduced in [39], [40] for the analysis of large arrays of nonlinear photovoltaic units and later used for implementing a diode-based audio ring modulator without reactances [8]. The convergence analysis of SIM offered in [8], [39], also discusses how to properly vary the free parameters (port resistances) of the WD structure in order to speed up convergence. SIM is able to solve circuits with an arbitrary number N_{nl} of 2-terminal nonlinear elements using N_{nl} independent one-dimensional NR solvers instead of one N_{nl}-dimensional NR solver. This implies several desirable features that greatly differentiate SIM from techniques based on multi-dimensional iterative solvers [29], [32]: greater robustness; guaranteed convergence when working with monotonically increasing $i - v$ nonlinearities such as diodes [8]); greater efficiency; and the possibility of solving the nonlinearities in a parallel fashion [39]. For all these reasons, SIM turns out to be particularly promising for Virtual Analog applications and it is worth extending its applicability to a wider class of nonlinear circuits. As SIM has been applied solely to circuits with no reactances, in order for it to be palatable for Virtual Analog modeling, it becomes important to extend its applicability to *dynamic* nonlinear circuits.

Most WD implementations of dynamic circuits presented in the literature use the trapezoidal discretization method with fixed sampling step for approximating the continuous-time

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derivative that appears in the constitutive equations of dynamic elements [1]. A good property of the trapezoidal method is that it is A-stable [41]. In addition, while digital implementations of dynamic linear circuits based on the trapezoidal rule generally result in implicit equations in the Kirchhoff domain [42], their WD description can be made explicit, after applying appropriate rules of adaptation [1].

Despite the excellent properties of the trapezoidal rule with fixed sampling step, alternate discretization techniques are often preferable. For example, the use of an adaptive sampling step, which is quite common in simulation software such as SPICE [42], [43], could significantly alleviate inaccuracies, particularly in the proximity of sudden signal amplitude variations, and especially when dealing with stiff systems (e.g. nonlinear relaxation oscillators); or could speed up simulations in presence of smooth signal variations. As a matter of fact, discretization methods other than the trapezoidal rule turn out to be preferable in many situations [44]. For example, the Backward Euler method can be fruitfully combined with the trapezoidal rule for implementing circuits with switches or for computing the first samples of simulations with uncertain initial conditions. Also, the use of higher-order discretization methods, such those based on the Backward Differentiation Formulas (BDF) (also known as Gear formulas) [45], are often opted for to achieve higher accuracy.

Although the idea of exploring different discretization methods in the WD domain is not new, there are surprisingly very few publications that address this topic. Some extensions of the traditional WD approach, which explore certain linear multi-step discretization methods with fixed sampling step are proposed in [46], [47], [48, pp. 33–47], and the use of passive Runge-Kutta methods in the WD domain is discussed in [49]–[52]. However, only a handful of publications [53], [54] address the problem of managing discretization methods with variable step-size in WD structures.

In this article, we propose an alternative approach to those presented in [53] and [54] for modeling dynamic nonlinear circuits in the WD domain using arbitrary Linear Multi-Step Discretization Methods (LMSDMs) with adaptive step-size as defined in [42]. The approach is based on digital representations of dynamic elements (e.g., capacitors and inductors) through *companion models*, i.e., Thévenin or Norton equivalent models, which vary according to the used discretization method [42], [55]. Such representations facilitate the derivation of optimal adaptation conditions for capacitors and inductors at each sampling time. Moreover, Thévenin or Norton equivalents allow us to treat dynamic elements as time-varying resistive voltage or current sources, respectively. This fact makes the proposed modeling approach particularly suitable to be used in conjunction with SIM [8] for solving dynamic circuits with multiple one-port nonlinearities, without the need of designing fictitious delays and resorting to the multi-dimensional WDF formalism as done in [38].

The article is organized as follows. Section II provides a background on the modeling of connection networks and memoryless one-ports in WD structures. Section III presents general WD models of capacitors and inductors based on LMSDMs with variable step-size, along with their properties. In Section IV the general WD models in Section III are applied to specific LMSDMs. Section V discusses the WD implementation of a class of nonlinear circuits employing the WD models presented in Section III. In particular, an extension of the applicability of SIM to dynamic circuits with multiple one-port nonlinearities is presented. In Section VI, WD implementations of a linear filter, a nonlinear Van Der Pol oscillator and a nonlinear ring modulator employing different LMSDMs are presented. Section VII concludes this article.

II. Background on Wave Digital Structures

In the WD domain, the topology and the elements of the reference circuit are typically modeled separately, using input/output blocks characterized by scattering relations. The derived blocks are then connected together through port connections and the WD structure is derived. In this Section, we briefly review how to compute the scattering matrices representing arbitrary reciprocal connection networks, i.e., topological interconnections possibly incorporating ideal transformers, in the WD domain [8], [39], [56], [57]. The reader who might be interested in the WD modeling of connection networks embedding both reciprocal and non-reciprocal linear elements, e.g., controlled sources, nullors or gyrators, is referred to [58]. In the following, we also briefly discuss the WD modeling of memoryless linear and nonlinear one-ports [1], [2].

A. Modeling Connection Networks

A N-port reciprocal connection network is characterized by the following pair of equations

$$\mathbf{v} = \mathbf{Q}^T \mathbf{v}_\mathrm{t} \ , \quad \mathbf{j} = \mathbf{B}^T \mathbf{j}_\mathrm{l} \ , \tag{1}$$

where the superscript ^{T} indicates matrix/vector transposition, $\mathbf{v} = [v_1, \ldots, v_N]^T$ is the column vector of all port voltages, $\mathbf{j} = [j_1, \ldots, j_N]^T$ is the column vector of all port currents, $\mathbf{v}_\mathrm{t}$ is a column vector of size q, $1 \leq q < N$, collecting independent port voltages, $\mathbf{j}_\mathrm{l}$ is a column vector of size p, $p = N - q$, collecting independent port currents. Matrices $\mathbf{Q}$ and $\mathbf{B}$ are generalizations of the fundamental cut-set matrix and fundamental loop matrix, respectively, as explained in [8], [56], [57], and they satisfy the orthogonality property $\mathbf{B}\mathbf{Q}^T = \mathbf{0}$, where $\mathbf{0}$ is a zero matrix of proper size. According to (1), each port voltage in $\mathbf{v}$ is expressed as a linear combination of the q independent port voltages collected in $\mathbf{v}_\mathrm{t}$, while each port current in $\mathbf{j}$ is expressed as a linear combination of the p independent port currents collected in $\mathbf{j}_\mathrm{l}$ [57].

The implementation of the connection network in the WD domain is a scattering junction characterized by a scattering matrix, which in turn can be expressed as a function of $\mathbf{Q}$ or $\mathbf{B}$. In order to define this scattering matrix, let us first consider the following port-wise definition of wave variables introduced by Fettweis [1]

$$\mathbf{a}_\mathrm{J} = \mathbf{v} + \mathbf{Z}\mathbf{j} \ , \qquad \mathbf{b}_\mathrm{J} = \mathbf{v} - \mathbf{Z}\mathbf{j} \ , \tag{2}$$

where $\mathbf{a}_\mathrm{J} = [a_{\mathrm{J}1}, \ldots, a_{\mathrm{J}N}]^T$ is the vector of incident waves (entering the WD junction), $\mathbf{b}_\mathrm{J} = [b_{\mathrm{J}1}, \ldots, b_{\mathrm{J}1}]^T$ is the vector

of reflected waves (exiting the WD junction), while the non-zero entries of the diagonal matrix $\mathbf{Z} = \text{diag}[Z_1, \ldots, Z_N]$ are free parameters called port resistances.

Wave variables defined in (2) are usually referred to as *voltage waves*, since their unit of measure is volt. Despite the definition in (2) is the most widespread, alternative definitions of waves, characterized by different units of measure [48], [57]–[59] and more than one free parameter per port [36], [57] have been discussed in the literature.

Incident and reflected waves are linked by the scattering relation

$$\mathbf{b}_\text{J} = \mathbf{S}\mathbf{a}_\text{J} \,, \tag{3}$$

where $\mathbf{S}$ is a $N \times N$ scattering matrix. As shown in [8], [39], [56], [57], $\mathbf{S}$ can be computed using one of the following two expressions

$$\mathbf{S} = 2\mathbf{Q}^T \left(\mathbf{Q}\mathbf{Z}^{-1}\mathbf{Q}^T\right)^{-1} \mathbf{Q}\mathbf{Z}^{-1} - \mathbf{I} \,, \tag{4}$$

$$\mathbf{S} = \mathbf{I} - 2\mathbf{Z}\mathbf{B}^T \left(\mathbf{B}\mathbf{Z}\mathbf{B}^T\right)^{-1} \mathbf{B} \,, \tag{5}$$

where $\mathbf{I}$ is the $N \times N$ identity matrix. Looking at equations (4) and (5), we notice that one of the two equations might be computationally less expensive to use, depending on whether the number of independent port voltages q is larger or smaller than the number of independent port currents p. In fact, as the sizes of the matrices $\mathbf{Q}$ and $\mathbf{B}$ are $q \times N$ and $p \times N$, respectively, eq. (4) involves the inversion of a $q \times q$ matrix, while eq. (5) involves the inversion of a $p \times p$ matrix.

B. Modeling One-port Memoryless Circuit Elements

The mapping between the WD variables of a one-port memoryless circuit element is derived by considering its constitutive equation in the Kirchhoff domain, which describes the relation between its port voltage v and its port current i, and then by applying the transformation

$$v = (a+b)/2 \quad , \qquad i = (a-b)/(2Z) \quad , \tag{6}$$

where a is the incident voltage wave (input), b is the reflected voltage wave (output), and Z is the port resistance [1]. The following two useful hybrid relations can be easily derived from (6)

$$i = (a-v)/Z \,, \tag{7}$$

$$b = 2v - a \,. \tag{8}$$

Here are two examples of interest: the WD implementation of linear resistive voltage sources and that of nonlinear diodes.

1) Resistive voltage sources and linear resistors: The constitutive equation of a resistive voltage source is $v = V_\text{g} + R_\text{g} i$, where V_g is the generator and R_g is its series resistance. The corresponding wave mapping, derived according to (6), is [1]

$$b = \frac{R_\text{g} - Z}{R_\text{g} + Z} a + \frac{2Z}{R_\text{g} + Z} V_\text{g} \,. \tag{9}$$

If the free parameter Z is set to R_g, the resistive voltage source is said to be *adapted*, as the instantaneous dependency between a and b is eliminated, and the wave mapping becomes simply $b = V_\text{g}$. Notice that, setting $V_\text{g} = 0$, (9) reduces to the wave mapping of an adapted resistor with resistance R_g.

2) Diodes: Let us consider the *extended Shockley diode model* presented in [8] and characterized by the nonlinear implicit equation

$$f(v,i) = I_\text{s}\left(\exp\left(\frac{v - R_\text{s} i}{\eta V_\text{t}}\right) - 1\right) + \frac{v - R_\text{s} i}{R_\text{p}} - i = 0 \tag{10}$$

where I_s is the saturation current, η is the ideality factor, V_t is the thermal voltage, while R_s and R_p are the series resistance and the shunt resistance of the p-n junction, respectively. As (10) is a transcendental equation, the derivation of a wave mapping is not straightforward. A closed-form scattering relation involving the Lambert function can be found using the approach described in [28]. Another possible efficient approach, which uses a one-dimensional Newton-Raphson (NR) solver, is explained in [8] and reported hereafter. If we substitute (7) in (10) we obtain

$$h(v) = I_\text{s}\left(e^{\frac{v(Z+R_\text{s}) - a R_\text{s}}{\eta V_\text{t} Z}} - 1\right) + \frac{v(Z + R_\text{p} + R_\text{s}) - a(R_\text{p} + R_\text{s})}{Z R_\text{p}}$$

and its derivative $h'(v)$ with respect to v,

$$h'(v) = \frac{I_s(Z + R_\text{s})}{\eta V_\text{t} Z} e^{\frac{v(Z+R_\text{s}) - a R_\text{s}}{\eta V_\text{t} Z}} + \frac{Z + R_\text{p} + R_\text{s}}{Z R_\text{p}} \,.$$

Given a, the nonlinear equation $h(v) = 0$ is iteratively solved for v by applying the NR update equation

$$v^{(\iota)} = v^{(\iota-1)} - \frac{h(v^{(\iota-1)})}{h'(v^{(\iota-1)})} \quad , \tag{11}$$

where the superscript between brackets is the iteration index and $\iota \geq 1$. Once the convergence condition $|v^{(\iota)} - v^{(\iota-1)}| < \epsilon_\text{NR}$ is met, ϵ_NR being a small tolerance (e.g. $\epsilon_\text{NR} = 10^{-10}$), the solver stops and the port voltage is set to $v = v^{(\iota)}$, so that the reflected wave b can be computed using (8). As the diode is nonlinear, unlike the resistive voltage source, it cannot be adapted, i.e. the instantaneous dependency between a and b cannot be eliminated [2].

III. General WD Models of Dynamic Elements based on LMSDMs

In this Section we show how to derive WD models of dynamic elements based on general LMSDMs with variable step-size [42]. The derivation is based on companion models [42], [55], also known as *associated discrete circuit models* [60], for dynamic elements, which are Thévenin or Norton equivalents whose parameters change at every sample. The Thévenin equivalent model is a resistive voltage source characterized by the following equation in the discrete-time domain

$$v[k] = R_\text{e}[k] i[k] + V_\text{e}[k] \tag{12}$$

where the index $k \geq 1$ in square brackets refers to the kth sample, $v[k]$ and $i[k]$ are the discrete-time port signals, $V_\text{e}[k]$ is the generator and $R_\text{e}[k]$ is the series resistance. The Norton equivalent model, instead, is a current source with parallel resistor characterized by

$$i[k] = G_e[k] v[k] + I_\text{e}[k] \tag{13}$$

where $I_\text{e}[k]$ is the current generator, $G_\text{e}[k]$ is the Norton conductance. Thévenin and Norton equivalent models that refer to the same element are related by

$$G_\text{e}[k] = 1/R_\text{e}[k] \,, \qquad I_\text{e}[k] = -G_\text{e}[k] V_\text{e}[k] \,. \tag{14}$$

Graphical representations of Thévenin and Norton equivalent models are shown in Fig. 1(a) and in Fig. 1(b), respectively.

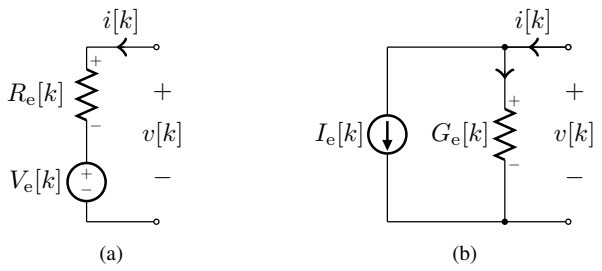


Fig. 1. Companion models of capacitors and inductors in the discrete-time domain. Fig. 1(a): Thévenin equivalent model. Fig. 1(b): Norton equivalent model.

In the discrete-time domain, the transformation of WD port variables to Kirchhoff port variables, already defined in (6), can be rewritten as

$$v\,[k] = \frac{a[k] + b[k]}{2} \quad , \quad i[k] = \frac{a[k] - b[k]}{2Z[k]} \quad , \tag{15}$$

where $a[k]$ and $b[k]$ are the discrete-time wave variables and $Z[k]$ is the port resistance depending on k. The inverse transformation of (15) is given by

$$a[k] = v[k] + Z[k]i[k] \quad , \quad b[k] = v[k] - Z[k]i[k] \ . \tag{16}$$

Similarly to what done in Subsection II-B, substituting (15) in (12) we get the wave mapping of the Thévenin equivalent

$$b\,[k] = \frac{R_\mathrm{e}\,[k] - Z[k]}{R_\mathrm{e}\,[k] + Z[k]} a[k] + \frac{2Z[k]}{R_\mathrm{e}\,[k] + Z[k]} V_\mathrm{e}[k] \ . \tag{17}$$

In case of adaptation we can write

$$b[k] = V_\mathrm{e}[k] \ , \ \text{if} \ Z[k] = R_\mathrm{e}[k] \ . \tag{18}$$

Similarly, by substituting (15) in (12) we obtain the wave mapping of the Norton equivalent

$$b\,[k] = \frac{1 - Z[k]G_\mathrm{e}[k]}{1 + Z[k]G_\mathrm{e}[k]} a[k] - \frac{2Z[k]}{1 + Z[k]G_\mathrm{e}[k]} I_\mathrm{e}[k] \tag{19}$$

In case of adaptation, eq. (19) simplifies to

$$b[k] = -I_\mathrm{e}[k]/G_\mathrm{e}[k] \ , \ \text{if} \ Z[k] = 1/G_\mathrm{e}[k] \ . \tag{20}$$

In the rest of this Section, we show how general WD models of capacitors and inductors based on a LMSDM can be derived by simply expressing the Thévenin equivalent parameters $V_\mathrm{e}[k]$ and $R_\mathrm{e}[k]$, or the Norton equivalent parameters $I_\mathrm{e}[k]$ and $G_\mathrm{e}[k]$, as functions of the past values of port signals, the coefficients of the discretization method, the variable step-size and the capacitance/inductance. It follows that WD realizations of capacitors and inductors based on a LMSDM can be obtained simply by implementing in the WD domain time-varying resistive voltage or current sources as those shown in Fig. 1; i.e., applying the scattering relations (17) or (19), respectively. In case of adaptation, the simplified scattering relations (18) or (20) can be directly used.

A. Capacitors

The constitutive equation of a capacitor of capacitance C in the continuous-time domain is

$$i(t) = C\frac{dv(t)}{dt} \tag{21}$$

where $v(t)$ and $i(t)$ are the continuous-time port signals, and t is the time variable in seconds. After applying a general LMSDM of order M with variable step-size [42], [60], the discrete-time version of (21) becomes

$$v[k] = \sum_{m=1}^{M} \mu_m[k]v[k-m] + \frac{h[k]}{C} \sum_{m=0}^{M} \eta_m[k]i[k-m] \tag{22}$$

where $\mu_1[k], \ldots, \mu_M[k]$ and $\eta_0[k], \eta_1[k], \ldots, \eta_M[k]$ are real coefficients, whose design depends on the chosen LMSDM. $h[k]$ is the variable step-size, which is defined as

$$h[k] = t_k - t_{k-1} \tag{23}$$

where t_k is the current sampling time and t_{k-1} is the previous one. Notice that, as $h[k]$ is assumed to be variable, we could have $h[k] \neq h[k-1]$ for each k.

Finding the Thévenin equivalent (12) of the discrete-time capacitor model (22) yields

$$R_\mathrm{e}[k] = \eta_0[k]\frac{h[k]}{C} \ , \tag{24}$$

$$V_\mathrm{e}[k] = \sum_{m=1}^{M} \eta_m[k]\frac{h[k]}{C} i[k-m] + \mu_m[k]v[k-m] \ . \tag{25}$$

The wave mapping of a WD capacitor can now be obtained by just substituting (24) and (25) in (17), or directly in (18), if the scattering relation of an adapted WD capacitor is needed.

Similarly, by equating (22) and (13) the following closed-form expressions of the Norton equivalent parameters are derived

$$G_\mathrm{e}\,[k] = \frac{C}{\eta_0[k]h[k]} \ , \tag{26}$$

$$I_\mathrm{e}[k] = \frac{-1}{\eta_0[k]} \left(\sum_{m=1}^{M} \mu_m[k]\frac{C}{h[k]} v[k-m] + \eta_m[k]i[k-m] \right) . \tag{27}$$

In this case, the wave mapping of a WD capacitor is obtained by just substituting (26) and (27) in (19), or directly in (20), if the scattering relation of an adapted WD capacitor is needed.

B. Inductors

The constitutive equation of an inductor with inductance L in the continuous-time domain is

$$v(t) = L\frac{di(t)}{dt} \ . \tag{28}$$

After applying a general LMSDM of order M with variable step-size [42], [60], the discrete-time version of (28) becomes

$$i[k] = \sum_{m=1}^{M} \mu_m[k]i[k-m] + \frac{h[k]}{L} \sum_{m=0}^{M} \eta_m[k]v[k-m] \ , \tag{29}$$

where $\mu_1[k], \ldots, \mu_M[k]$ and $\eta_0[k], \eta_1[k], \ldots, \eta_M[k]$ are the same real coefficients appearing in eq. (22) and the variable step-size $h[k]$ is defined as in eq. (23).

Equating (29) and (13) the following closed-form expressions of the Thévenin equivalent parameters are obtained

$$R_{\mathrm{e}}[k] = \frac{L}{\eta_0[k] h[k]} \ , \tag{30}$$

$$V_{\mathrm{e}}[k] = \frac{-1}{\eta_0[k]} \left(\sum_{m=1}^{M} \mu_m[k] \frac{L}{h[k]} i[k-m] + \eta_m[k] v[k-m] \right) . \tag{31}$$

The wave mapping of a WD inductor is obtained substituting (30) and (31) in (17), or directly in (18), if the scattering relation of an adapted WD inductor is needed.

Similarly, by equating (29) and (13) the following closed-form expressions of the Norton equivalent parameters are obtained

$$G_{\mathrm{e}}[k] = \eta_0[k] \frac{h[k]}{L} \ , \tag{32}$$

$$I_{\mathrm{e}}[k] = \sum_{m=1}^{M} \eta_m[k] \frac{h[k]}{L} v[k-m] + \mu_m[k] i[k-m] \ . \tag{33}$$

The wave mapping of a WD inductor is obtained by substituting (32) and (33) in (19), or directly in (20), if the scattering relation of an adapted WD inductor is needed.

C. On the possibility of performing adaptation

General adaptation conditions for WD models of reactances based on LMSDMs are provided in (18) and (20). The applicability of such adaptation conditions, however, depends on the LMSDM that we are dealing with. The following two rules state when and how adaptation conditions can be set.

Rule I. If $\eta_0[k] \neq 0$, capacitors or inductors can be represented by Thévenin equivalents with non-zero series resistances at each sampling step; therefore, a WD realization can always be derived in which there is not an instantaneous dependency between the incident wave and the reflected wave, provided that adaptation is performed, according to eq. (18) or eq. (20).

Rule II. If $\eta_0[k] = 0$, capacitors do not admit a Norton representation (see eq. (26) and eq. (27)), while they admit a representation based on a Thévenin equivalent with zero series resistance, i.e., an ideal voltage source (see eq. (24) and eq. (25)); dually, inductors admit only a representation based on a Norton equivalent with zero parallel admittance, i.e., an ideal current source (see eq. (32) and eq. (33)). Therefore, when $\eta_0[k] = 0$, adaptation cannot be performed in either cases (capacitor or inductors).

It is worth noticing that the aforementioned rules are in line with the considerations drawn in the doctoral dissertation by Werner [48, pp. 33–47], where it is shown that capacitors and inductors can be adapted only if implicit discretization methods are used; while, when explicit discretization methods, like Forward Euler, are chosen, adaptation cannot be performed.

IV. WD Models of Dynamic Elements based on Specific LMSDMs

A. LMSDMs with Fixed Step-Size

Table I presents a characterization of discrete models of capacitors and inductors based on some LMSDMs with fixed step-size, used for implementing dynamic circuit networks [42], showing their weighting coefficients. For each indicated LMSDM, all the weighting coefficients $\eta_m[k]$ and $\mu_m[k]$ not shown in Table I are assumed to be equal to 0. As the time-step size in Table I is assumed to be fixed, the coefficient values are fixed as well. The last column of Table I indicates whether WD models of capacitors and inductors based on a specific LMSDM can be adapted, eliminating the instantaneous dependency between the incident wave and the reflected wave. Quite naturally, the most interesting LMSDMs in our context are those that lead to WD models where adaptation can be performed. In the following, we focus on some WD models of the sort, considering the more general scenario in which the step-size is assumed to be variable.

B. Trapezoidal Method

The non-zero coefficients $\eta_0[k]$, $\eta_1[k]$ and $\mu_1[k]$ of the trapezoidal method in the variable step-size scenario are the same as reported in Table I and used in the fixed step-size case [42]. It follows that the adaptation condition for a *WD capacitor* is

$$Z[k] = \frac{h[k]}{2C} \ . \tag{34}$$

Hence, substituting (25) in (18) and then expressing Kirchhoff variables in terms of wave variables according to (15), the scattering relation becomes

$$b[k] = \frac{a[k-1]}{2} \left(1 + \frac{h[k]}{h[k-1]} \right) + \frac{b[k-1]}{2} \left(1 - \frac{h[k]}{h[k-1]} \right) . \tag{35}$$

The adaptation condition for a *WD inductor*, instead, is

$$Z[k] = \frac{2L}{h[k]} \ . \tag{36}$$

Hence, substituting (31) in (18) and then expressing Kirchhoff variables in terms of wave variables according to (15), the scattering relation becomes

$$b[k] = \frac{a[k-1]}{-2} \left(1 + \frac{h[k-1]}{h[k]} \right) + \frac{b[k-1]}{-2} \left(1 - \frac{h[k-1]}{h[k]} \right) . \tag{37}$$

When $h[k-1] = h[k]$, scattering relations (35) and (37) reduce to the ones employed in traditional WD filters [1].

C. Backward Euler Method

The non-zero coefficients $\eta_0[k]$ and $\mu_1[k]$ of the Backward Euler (BE) method in the variable step-size scenario are the same reported in Table I and used in the fixed step-size case [42]. It follows that the adaptation condition for a *WD capacitor* is

$$Z[k] = \frac{h[k]}{C} \ , \tag{38}$$

TABLE I
CHARACTERIZATION OF WD MODELS OF CAPACITORS AND INDUCTORS BASED ON LMSDMS WITH FIXED STEP-SIZE

Method	Coefficients								Adaptation possible (yes/no)
	$\eta_0[k]$	$\eta_1[k]$	$\eta_2[k]$	$\eta_3[k]$	$\mu_1[k]$	$\mu_2[k]$	$\mu_3[k]$	$\mu_4[k]$	
Backward Euler	1	0	0	0	1	0	0	0	yes
Trapezoidal	1/2	1/2	0	0	1	0	0	0	yes
Adams-Moulton 2	5/12	2/3	-1/12	0	1	0	0	0	yes
Adams-Moulton 3	3/8	19/24	-5/24	1/24	1	0	0	0	yes
BDF 2	2/3	0	0	0	4/3	-1/3	0	0	yes
BDF 3	6/11	0	0	0	18/11	-9/11	2/11	0	yes
BDF 4	12/25	0	0	0	48/25	-36/25	16/25	-3/25	yes
Forward Euler	0	1	0	0	1	0	0	0	no
Adams-Bashforth 2	0	1	0	0	3/2	-1/2	0	0	no
Adams-Bashforth 3	0	1	0	0	23/12	-4/3	5/12	0	no
Adams-Bashforth 4	0	1	0	0	55/24	-59/24	37/24	-3/8	no

and, according to (18) and (25), the scattering relation becomes

$$b[k] = \frac{a[k-1] + b[k-1]}{2} \ . \tag{39}$$

The adaptation condition for a *WD inductor*, instead, is

$$Z[k] = \frac{L}{h[k]} \ , \tag{40}$$

and, according to (18) and (31), the scattering relation becomes

$$b[k] = \frac{h[k-1]}{2h[k]} \left(b[k-1] - a[k-1]\right) \ . \tag{41}$$

D. Higher-Order Backward Differentiation Formulas

BDF methods of order $M > 1$, in the variable step-size scenario, are characterized by non-fixed coefficients depending on the actual step-sizes, hence the coefficients provided in Table I are not appropriate in this case [42]. In this Subsection, we provide general WD models of adapted capacitors and inductors based on BDF methods. Then, we derive closed-form expressions for computing the coefficients needed in BDF 2, BDF 3 and BDF 4, when the step-size is assumed to be variable.

Applying a BDF of order M and setting the adaptation condition $Z[k] = \eta_0[k]h[k]/C$, the scattering relation of a *WD capacitor* becomes

$$b[k] = \sum_{m=1}^{M} \frac{\mu_m[k]}{2} \left(a[k-m] + b[k-m]\right) \tag{42}$$

Similarly, setting the adaptation condition $Z[k] = L/\left(\eta_0[k]h\left[k\right]\right)$, the scattering relation of a *WD inductor*, becomes

$$b[k] = \sum_{m=1}^{M} \frac{\mu_m[k]\eta_0[k-m]h\left[k-m\right]}{2\eta_0[k]h\left[k\right]} \left(b[k-m] - a[k-m]\right) . \tag{43}$$

The coefficients of a BDF of order M are computed as

$$\eta_0[k] = \frac{-1}{u_0[k]} \ , \ \mu_m[k] = \eta_0[k]u_m[k] \quad \text{with} \ \ 1 \leq m \leq M \tag{44}$$

where, in accordance with the procedure presented in [42], the parameters $u_m[k]$, with $0 \leq m \leq M$, are given by

$$\begin{bmatrix} u_0[k] \\ u_1[k] \\ u_2[k] \\ \vdots \\ u_M[k] \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \dots & 0 \\ 1 & 1 & 1 & \dots & 1 \\ 1 & \tau_2[k] & (\tau_2[k])^2 & \dots & (\tau_2[k])^M \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & \tau_M[k] & (\tau_M[k])^2 & \dots & (\tau_M[k])^M \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix} , \tag{45}$$

and the further parameters $\tau_j[k]$ are defined as

$$\tau_j[k] = \frac{h[k] + \sum_{m=1}^{j-1} h[k-m]}{h[k]} \ , \ \text{with} \ 1 < j \leq M \ . \tag{46}$$

Here follow closed-form expressions of the coefficients in the cases $M = 2$, $M = 3$ and $M = 4$. It is worth saying that such closed-form expressions for BDF 3 and BDF 4 are not available in [42].

1) Coefficients for BDF 2:

$$\eta_0[k] = \frac{\tau_2[k]}{\tau_2[k]+1} \ ,$$

$$\mu_1[k] = \eta_0[k]\frac{\tau_2[k]}{\tau_2[k]-1} \quad , \quad \mu_2[k] = \eta_0[k]\frac{1}{\tau_2[k](1-\tau_2[k])} \ .$$

2) Coefficients for BDF 3:

$$\eta_0[k] = \frac{\tau_2[k]\tau_3[k]}{\tau_2[k]+\tau_3[k]+\tau_2[k]\tau_3[k]} \ ,$$

$$\mu_1[k] = \eta_0[k]\frac{\tau_2[k]\tau_3[k]}{(\tau_2[k]-1)(\tau_3[k]-1)} \ ,$$

$$\mu_2[k] = \eta_0[k]\frac{\tau_3[k]}{\tau_2[k](\tau_2[k]-1)(\tau_2[k]-\tau_3[k])} \ ,$$

$$\mu_3[k] = \eta_0[k]\frac{\tau_2[k]}{\tau_3[k](1-\tau_3[k])(\tau_2[k]-\tau_3[k])} \ .$$

3) Coefficients for BDF 4:

$$\eta_0[k] = \frac{\tau_2[k]\tau_3[k]\tau_4[k]}{\tau_2[k]\tau_3[k]+\tau_2[k]\tau_4[k]+\tau_3[k]\tau_4[k]+\tau_2[k]\tau_3[k]\tau_4[k]} ,$$

$$\mu_1[k] = \eta_0[k]\frac{\tau_2[k]\tau_3[k]\tau_4[k]}{(\tau_2[k]-1)\left(\tau_3[k]-1\right)(\tau_4[k]-1)} \ ,$$

$$\mu_2[k] = \eta_0[k]\frac{\tau_3[k]\tau_4[k]}{\tau_2[k](\tau_3[k]-\tau_2[k])(\tau_2[k]-\tau_4[k])(\tau_2[k]-1)} \ ,$$

$$\mu_3[k] = \eta_0[k] \frac{\tau_2[k]\tau_4[k]}{\tau_3[k](\tau_2[k]-\tau_3[k])(\tau_3[k]-\tau_4[k])(\tau_3[k]-1)} \ ,$$

$$\mu_4[k] = \eta_0[k] \frac{\tau_2[k]\tau_3[k]}{\tau_4[k](\tau_4[k]-\tau_2[k])(\tau_3[k]-\tau_4[k])(\tau_4[k]-1)} \ .$$

E. Automatic Step-Size Variation

Different strategies can be used for automatically adapting the time-step size during the digital emulation of an audio circuit. The design of algorithms for the automatic change of the step-size strongly depends on the accuracy and efficiency requirements of the reference application. As a detailed discussion on the optimization criteria for step-size variation is beyond the scope of this article, here we simply mention that, algorithms that eventually change the step-size $h[k+1]$ at each sampling step $k+1$ with respect to $h[k]$, are usually based on the estimation of the *Local Truncation Error* (LTE) at each port connected to a dynamic element [43]. For instance, the LTE $e_n[k]$ associated to the BE discretization formula for a capacitor with capacitance C at port n is $e_n[k] \approx h^2[k]v_n''[k]/2$, where $v_n''[k]$ is the second order time derivative of the voltage across the capacitor evaluated at the time instant corresponding to the kth sample [43], and it can be approximated as $\hat{e}_n[k] = w_n[k](i_n[k] - i_n[k-1])$ with $w_n = h[k]/(2C)$. However, more advanced prediction algorithms could be employed for estimating the LTEs, which depend on the used LMSDM; see, e.g., [60] and [43] for a discussion on these aspects. Depending on the magnitude of the estimated LTEs, one might decide to: increase the step-size, i.e., set $h[k+1] = g_{\text{inc}}h[k]$, with $g_{\text{inc}} > 1$, if the estimated LTEs are sufficiently low; leave the step-size unchanged, i.e., set $h[k+1] = h[k]$; reduce the step-size, i.e., set $h[k+1] = g_{\text{red}}h[k]$, with $0 < g_{\text{red}} < 1$; or even repeat the computation of $i_n[k]$ with a reduced time-step $h[k]$, if the estimated LTEs are too large.

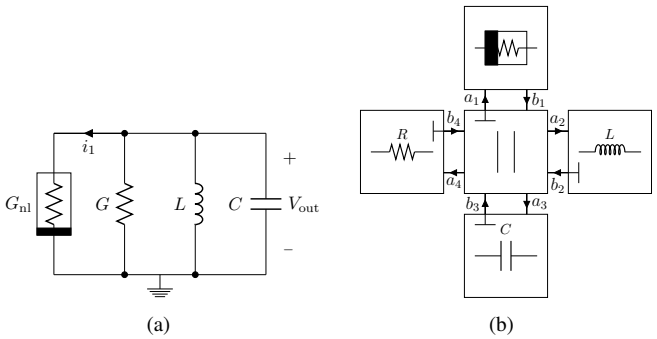
V. WD Implementation of Nonlinear Dynamic Circuits

In this Section, we discuss strategies for implementing nonlinear dynamic circuits in the WD domain. We focus our attention to circuits with one-port nonlinearities. We first revise a common efficient strategy for implementing WD structures with one nonlinear one-port, known since the publication of [2], in which all global delay-free loops are eliminated. We then show how, in the light of the results presented in the previous two Sections, the applicability of SIM [8], [39] can be extended to dynamic circuits with multiple nonlinear one-ports.

A. One Nonlinearity Case

Let us consider a WD multi-port junction describing the connection network of a circuit with one nonlinear element and a number of memoryless or dynamic linear elements. We also consider the scattering matrix characterizing the connection network, defined as in Section II. The free parameter (port resistance) of the junction port facing the nonlinear element is set in such a way that the corresponding diagonal entry of the scattering matrix becomes zero. This ensures that the junction port is reflection free, which means the instantaneous dependence between the incident wave and the reflected wave at that port is eliminated [2]. We assume that all the linear elements are adapted, according to the constraints provided in the previous Sections. Then, the WD elements are virtually connected to the WD junction by first forcing the reflected waves from the junction to be equal to the incident waves to the elements and vice-versa and then setting the port resistances of the junction to be equal to the port resistances of the WD elements, in a port-wise fashion [1]. Under these assumptions all the global delay-free loops due to the interconnections of circuit elements are eliminated, as already explained in [2] and, more recently, in [36]. It follows that, if look-up tables [3] or, more conveniently, canonical piecewise linear representations of functions [23] are used for computing the nonlinear wave mapping, the reference circuit is implemented in a *fully explicit* fashion. Alternatively, one-dimensional NR solvers can be used for solving the potentially implicit constitutive equation of the nonlinear element in the WD domain, without necessarily loosing robustness and efficiency, as explained in Subsection II-B.

As an example, Fig. 2(b) shows a WD structure corresponding to the oscillator with one nonlinear element in Fig. 2(a). We notice that port 1 of the WD junction (a 4-port parallel adaptor) is adapted, along with all the linear elements of the WD structure.



(a) (b)

Fig. 2. Van Der Pol oscillator circuit in Fig. 2(a) and corresponding WD structure in Fig. 2(b).

B. Multiple Nonlinearities Case: Scattering Iterative Method

As discussed in [36] and references therein, the presence of more than one nonlinear element in a WD structure results in unavoidable delay-free loops, i.e., a set of implicit equations involving port variables of different nonlinear elements that make the digital structure not computable without resorting to iterative solvers. In [8], [39] a relaxation method, called SIM, which efficiently solves circuits with multiple one-port nonlinearities in the WD domain is presented. However, the circuits considered in [8], [39] do not contain dynamic elements. Here we show how the approach for modeling inductors and capacitors presented in Section III and Section IV allows to easily handle dynamic nonlinear circuits using SIM.

Let us assume, without loss of generality, that the number of nonlinear elements is $N_{\text{nl}} < N$ and that they are connected

to the first N_{nl} ports of the WD junction. Let us collect waves incident to and reflected from the elements in the two vectors $\mathbf{a}[k] = [a_1[k], \ldots, a_N[k]]^T$ and $\mathbf{b}[k] = [b_1[k], \ldots, b_N[k]]^T$, respectively, where the argument k in square brackets indicates signals at kth sampling step. The connection of the elements to the junction implies that the vector of port voltages $\mathbf{v}$ of the elements is the same defined in Subsection II-A, while the vector of port currents of the elements $\mathbf{i}[k] = [i_1[k], \ldots, i_N[k]]^T$ satisfies $\mathbf{i}[k] = -\mathbf{j}[k]$. It follows that $\mathbf{a}[k] = \mathbf{b}_{\text{J}}[k]$ and $\mathbf{b}[k] = \mathbf{a}_{\text{J}}[k]$. SIM is applied at each sampling step k and it requires to perform the following four stages.

1) Initialization: each free parameter $Z_n[k]$, with $1 \leq n \leq N$, is set as close as possible to the *slope of the tangent line* passing through the actual operating point on the $i-v$ curve of the nth one-port, i.e., the series resistance of its Thévenin equivalent.

According to the considerations in Section III, both memoryless and dynamic linear elements can be described by Thévenin (or Norton) equivalents whose parameters are independent of the coordinates of the actual operating point. It follows that in those cases free parameters can be set in an optimal fashion, i.e. $Z_n[k] = R_{\text{e}n}[k]$, where $R_{\text{e}n}[k]$ is the Thévenin resistance of the linear element connected to the nth port of the junction, with $N_{\text{nl}} < n \leq N$.

Dealing with nonlinear elements, instead, the exact Thévenin equivalent parameters are not easy to derive in this stage, because they depend on the coordinates of the actual operating point. In fact, assuming each nonlinearity is characterized by a nonlinear equation $f_n(v_n, i_n) = 0$, mathematically, the Thévenin series resistance would be given by

$$R_{\text{e}n}[k] = -\frac{\partial f_n\left(v_n[k], i_n[k]\right)/\partial i_n}{\partial f_n\left(v_n[k], i_n[k]\right)/\partial v_n} \quad , \quad 1 \leq n \leq N_{\text{nl}} \ . \tag{47}$$

However, the coordinates of the actual operating point, $v_n[k]$ and $i_n[k]$, are unknown. Therefore, the best we can do is to perform a prediction of the desired slope $R_{\text{e}n}[k]$, based on its values at previous sampling steps.

In the light of this, an effective initialization is performed setting

$$\begin{aligned}\mathbf{Z}[k] = \text{diag}\,[&R_{\text{e}1}[k-1], \ldots, R_{\text{e}N_{\text{nl}}}[k-1], \\ &R_{\text{e}N_{\text{nl}}+1}[k], \ldots, R_{\text{e}N}[k]] \quad ,\end{aligned}$$

where $\mathbf{Z}[k]$ is the diagonal matrix of free parameters (port resistances). Vectors of port voltages and incident waves are set to initial guesses $\mathbf{a}^{(0)}[k] = \left[a_1^{(0)}[k], \ldots, a_N^{(0)}[k]\right]^T$ and $\mathbf{v}^{(0)}[k] = \left[v_1^{(0)}[k], \ldots, v_N^{(0)}[k]\right]^T$, given by

$$\begin{aligned}&\mathbf{a}^{(0)}[k] = [a_1[k-1], \ldots, a_N[k-1]]^T \ , \\ &\mathbf{v}^{(0)}[k] = \tfrac{1}{2}\,[2v_1[k-1], \ldots, 2v_{N_{\text{nl}}}[k-1], \\ &a_{N_{\text{nl}}+1}[k-1] + V_{\text{e}N_{\text{nl}}+1}[k], \ldots, a_N[k-1] + V_{\text{e}N}[k]]^T \ ,\end{aligned}$$

where $V_{\text{e}n}[k]$ with $N_{\text{nl}} < n \leq N$ are the Thévenin voltage sources of linear elements.

2) Local Scattering Stage: the reflected wave from each memoryless or dynamic linear element is given by $b_n[k] = V_{\text{e}n}[k]$ with $N_{\text{nl}} < n \leq N$, independently of the values of incident wave. Reflected waves from nonlinear elements, instead, depend on the incident waves. It follows that the vector of reflected waves $\mathbf{b}^{(\gamma)}[k]$ at iteration $\gamma \geq 1$ of SIM, where the superscript in round brackets indicates the iteration index, is given by

$$\mathbf{b}^{(\gamma)}[k] = \left[b_1^{(\gamma)}[k], \ldots, b_{N_{\text{nl}}}^{(\gamma)}[k], V_{\text{e}N_{\text{nl}}+1}[k], \ldots, V_{\text{e}N}[k]\right]^T \tag{48}$$

where, in turn,

$$b_n^{(\gamma)}[k] = 2v_n^{(\gamma)}[k] - a_n^{(\gamma-1)}[k] \ , \ \text{with} \ 1 \leq n \leq N_{\text{nl}} \ . \tag{49}$$

The way of computing $v_n^{(\gamma)}[k]$ depends on the actual considered nonlinear element. For instance, if a diode characterized by the extended Shockley diode model is considered, the one-dimensional NR solver described in Subsection II-B can be used with initial guess $v_n^{(\gamma-1)}[k]$.

3) Global Scattering Stage: given $\mathbf{b}^{(\gamma)} = \left[b_1^{(\gamma)}, \ldots, b_N^{(\gamma)}\right]^T$, the vector of incident waves to the elements at iteration γ, $\mathbf{a}^{(\gamma)} = \left[a_1^{(\gamma)}, \ldots, a_N^{(\gamma)}\right]^T$, is given by

$$\mathbf{a}^{(\gamma)}[k] = \mathbf{S}[k]\mathbf{b}^{(\gamma)}[k] \tag{50}$$

where $\mathbf{S}[k]$ indicates the scattering matrix computed according to equations provided in Subsection II-A and using the diagonal matrix of free parameters $\mathbf{Z}[k]$.

4) Convergence Check: if the following convergence condition is met

$$\left\|\mathbf{a}^{(\gamma)}[k] - \mathbf{a}^{(\gamma-1)}[k]\right\|_2 < \epsilon_{\text{SIM}} \tag{51}$$

where ϵ_{SIM} is a small tolerance, e.g. $\epsilon_{\text{SIM}} = 10^{-6}$, the output port variables of SIM at sampling step k are set as: $\mathbf{a}[k] = \mathbf{a}^{(\gamma)}[k]$, $\mathbf{b}[k] = \mathbf{b}^{(\gamma)}[k]$ and $\mathbf{v}[k] = \mathbf{v}^{(\gamma)}[k]$. Conversely, if condition (51) is not satisfied the iteration index γ is incremented by one such that the local scattering stage and the global scattering stage are performed again. The local scattering stage, the global scattering stage and the convergence check are repeated up to convergence.

Discussion on Convergence: according to the theorem presented in [39] and restated in [8], convergence of SIM applied to a memory-less circuit with nonlinear one-ports, such as diodes with a constitutive equation like (10), is guaranteed when the connection network is reciprocal, the $i-v$ characteristic of each element is monotonically increasing and robust one-dimensional solvers are used in the local scattering stage to compute reflected waves from the WD one-port nonlinear elements. In this paper we consider more general consequences of the theorem in [39] on the analysis of nonlinear circuits with reactances. It turns out that if a discrete-time model based on LMSDM of a capacitor or an inductor can be represented as a Thévenin equivalent with positive series resistance, i.e., $\eta_0[k] > 0$, the corresponding $i-v$ characteristic at each time step k is monotonically increasing. Therefore, SIM converges when applied to circuits characterized by a reciprocal connection network, nonlinear memoryless one-ports with monotonically increasing $i-v$ characteristics and linear reactive elements discretized using LMSDMs with $\eta_0[k] > 0$. It is worth noticing that, in practice, convergence can be achieved even when SIM is applied to nonlinear circuits for which convergence is not ensured by a

theoretical analysis. As a matter of fact, convergence of other mainstream iterative solvers applied to nonlinear circuits, like multivariate NR methods, is not theoretically guaranteed in general.

VI. Examples of Application

A. A Linear Filter

As a first example of application of the proposed approach for modeling dynamic elements, let us consider the simple first-order filter in Fig. 3(a) and its WD realization [1] in Fig. 3(b). The analysis of a linear filter like the one in Fig. 3 allows us to compare the behavior of WD models of the capacitor based on different LMSDMs with an "exact" ground truth.

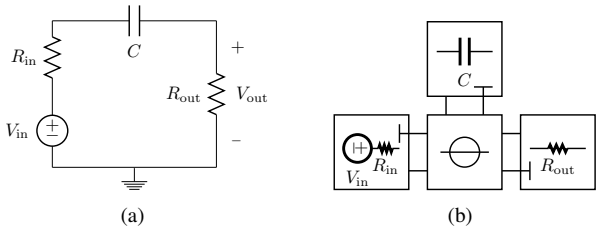


Fig. 3. Linear filter circuit in Fig. 3(a) and corresponding WD structure in Fig. 3(b).

In fact, we can express the time evolution of the voltage V_{out} across the resistor R_{out} in closed-form. Assuming that the voltage across the capacitor at $t = 0$ is zero, we have that

$$V_{\text{out}}(t) = V_{\text{in}} \frac{R_{\text{out}}}{R_{\text{tot}}} \, e^{-t/(R_{\text{tot}}C)} \,, \tag{52}$$

where V_{in} is a constant and $R_{\text{tot}} = R_{\text{in}} + R_{\text{out}}$. We set $V_{\text{in}} = 5$ V, $R_{\text{in}} = 12\ \Omega$, $R_{\text{out}} = 3\ \Omega$ and $C = 100\ \mu$F.

In a first experiment, the capacitor is implemented using three alternative discretization techniques: the traditional trapezoidal method, i.e., scattering relation (35) and adaptation condition (34), the BE method, i.e., scattering relation (39) and adaptation condition (38), and a combination of BE and trapezoidal in which BE is used to compute the first sample, while trapezoidal is used for the following samples. A fixed step-size $h[k] = 1/F_{\text{s}}$ sec with $F_{\text{s}} = 8$ kHz is employed. The errors with respect to the ground truth computed using (52) are shown in Fig. 4; the red line with asterisks refers to trapezoidal, the blue line with crosses refers to BE, while the green line with circles refers to the above combination. Despite trapezoidal is in general more accurate than BE, the error of the former at first samples is higher because the first sample is computed relying on a bad approximation of the derivative of the voltage across the capacitor at sampling time t_{k-1}. As shown in Fig. 4, a good strategy to cope with this problem is to use the BE method for computing the first sample and then switch to the trapezoidal method. In order to properly perform the switching between BE and trapezoidal maintaining adaptation, scattering relation (35) and adaptation condition (34) are used at the first sampling step, while scattering relation (39) and adaptation condition (38) are used for the following steps.

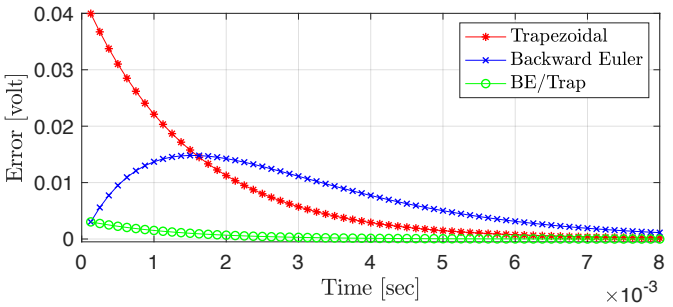


Fig. 4. WD implementations of the linear filter; comparison between three discretization methods with fixed step-size. The three lines represent the errors of the signals V_{out} w.r.t. the ground truth, referred to the implementations in which the trapezoidal method, the BE method and a combination of the two (i.e., BE for the first sample and then trapezoidal) are used.

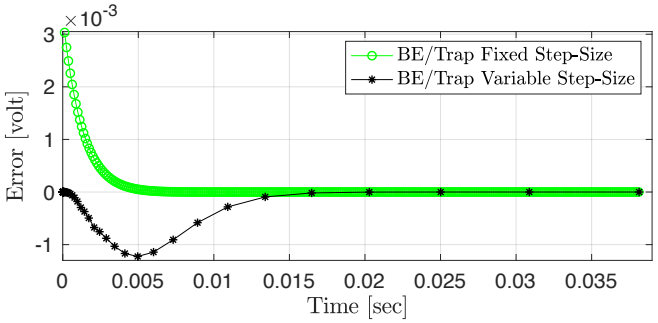


Fig. 5. WD implementation of the linear filter using a combination of BE and trapezoidal methods. A comparison between the fixed and the variable step-size cases is presented. The two lines represent the errors of the signals V_{out} w.r.t. the ground truth. The green line with circles refers to the fixed step-size case; the number of circles, i.e., 311, is the number of samples. The black line with asterisks refers to the variable step-size case; the number of asterisks, i.e., 54, is the number of samples. In both cases the MSE is 1.6×10^{-7}.

In a second experiment, we implement a new version of the above combination of BE and trapezoidal methods based on a variable step-size. We perform an ad hoc optimization of the step-sizes in order to match the mean squared error (MSE) of the fixed sampling step implementation considered in the previous experiment, i.e., 1.6×10^{-7}. We obtain an implementation with variable step-size employing 54 samples versus the 311 samples used in the fixed step-size case to simulate the same transient from $t = 0$ seconds to $t = 0.039$ seconds. This result demonstrates that the simulation of the transient can be performed almost six times faster using a variable step-size, while preserving the MSE of the fixed step-size case. Fig. 5 shows the evolution in time of the error; the kth green circle indicates the error referred to the kth sample in the fixed step-size case, while the kth black asterisk indicates the error referred to the kth sample in the variable step-size case. Notice that in the variable step-size case asterisks are dense at the beginning of the transient and increasingly sparse as time t increases, since the signal V_{out} varies less and less.

Finally, we performed Kirchhoff domain discrete-time simulations [42] of the simple circuit in Fig. 3(a), based on the same LMSDMs discussed in this Subsection, and we verified that the results are identical (up to numerical precision) to those obtained with the presented WD implementations.

B. Van Der Pol Oscillator

In this Subsection, we show how a variable step-size can be useful to improve the WD realization of a relaxation oscillator, like the Van Der Pol oscillator [61] in Fig. 2(a), preventing possible artifacts.

The circuit parameters are $R = 1/G = 260\ \Omega$, $L = 5.1$ mH and $C = 1.442\ \mu$F. The nonlinear conductor G_{nl} is characterized by

$$f(v,i) = i + \alpha v - \beta v^3 = 0\ ,$$

where α and β are two scalar coefficients. We set $\alpha = 0.2648$ and $\beta = 0.000976$.

The WD structure corresponding to the nonlinear circuit in Fig. 2(a) is represented in Fig. 2(b). First, a WD implementation of the oscillator employing the trapezoidal method with fixed step-size is validated, verifying that it matches with a corresponding Kirchhoff implementation based on nodal analysis and a NR solver. These two implementations are performed with an extremely high sampling frequency, i.e., $F_{\text{GT}} = 1024$ kHz, in order to obtain a reliable ground truth. Then, other WD implementations with fixed sampling rate $F_{\text{s}} = 96$ kHz and variable step-size are developed. The variable step-size is adapted according to the considerations about the estimated LTE discussed in Subsection IV-E. As a constraint in the process of adaptation of the step-size we impose that the average number of samples per period of the periodic output signal V_{out} matches the fixed step-size case, i.e., about 225 samples per period. Fig. 6(a) shows three versions of the V_{out} signal; the green line with circles refers to the ground truth, the blue line with circles refers to the WD implementation based on fixed sampling rate, $F_{\text{s}} = 96$ kHz, while the red line with asterisks refers to the WD implementation based on variable step-size. A portion of Fig. 6(a) is zoomed in Fig. 6(b), which clearly shows an artifact due to the abrupt change of signal amplitude and a consequent high LTE, characterizing the fixed step-size curve. Such an artifact, instead, is highly attenuated when the adaptive step-size is used, because samples with high estimated LTE are discarded and recomputed after reducing the step-size. We deduce that it is possible to obtain a WD implementation of the oscillator with variable step-size which employs the same average number of samples per period of the fixed step-size implementation ($F_{\text{s}} = 96$ kHz), but does not suffer from the same artifacts due to discretization errors.

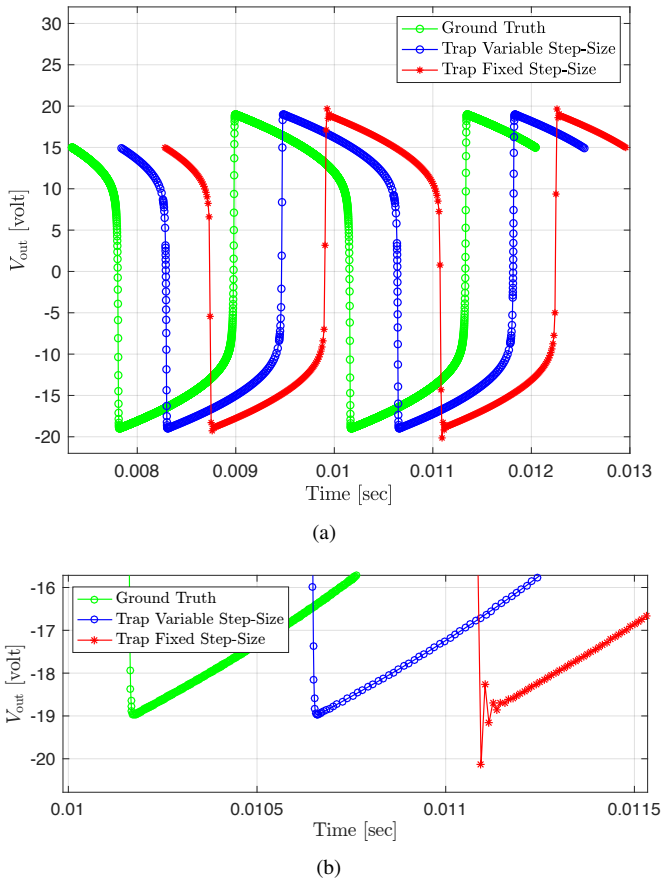


Fig. 6. WD implementations of the Van Der Pol oscillator; three lines indicate different versions of the output signal V_{out} (shifted in time for improving visibility). Two trapezoidal methods with fixed and variable step-size are compared in Fig. 6(a). The green line with circles indicates the ground truth. The blue line with circles refers to the variable step-size case. The red line with asterisks refers to the fixed step-size case. In both variable and fixed step-size cases the average number of samples per period is 225. Fig. 6(b) shows a zoomed detail of Fig. 6(a).

C. Dynamic Diode-based Ring Modulator

The dynamic digital model of the audio ring modulator circuit presented in [62], [63] is reported in Fig. 7. A WD implementation based on SIM of a similar circuit without inductors and capacitors is described in [8]. In this Subsection, we show that SIM can also be applied to the circuit in Fig. 7 containing dynamic elements and multiple nonlinear diodes, according to the considerations discussed in Subsection V-B. As in [8], the four diodes are assumed to be characterized by the nonlinear constitutive equation (10). We set the parameters of the diode model as $I_{\text{s}} = 10^{-9}$ nA, $\eta = 2.19$, $V_{\text{t}} = 26$ mV, $R_{\text{s}} = 1\ \text{m}\Omega$ and $R_{\text{p}} = 100\ \text{k}\Omega$. The turn ratios of the ideal transformers are $\theta/\mu = \gamma/\mu = \xi/\lambda = \tau/\lambda = 1/2$, where θ, γ, μ, ξ, τ and λ are the numbers of turns in each winding. The other parameters of the circuit are $L_{\text{A}} = L_{\text{B}} = 0.8$ H, $C_{\text{A}} = C_{\text{B}} = C_{\text{d}} = 1$ nF, $R_{\text{d}} = 50\ \Omega$, $R_{\text{in}} = 80\ \Omega$, $R_{\text{c}} = 1\ \Omega$, $R_{\text{out}} = 600\ \Omega$. In the following, we will assume that the input voltage signal and the carrier voltage signal are two sinusoids $V_{\text{in}}(t) = \sin(2\pi f_{\text{in}} t)$ and $V_{\text{c}}(t) = \sin(2\pi f_{\text{c}} t)$ with fundamental frequencies $f_{\text{in}} = 150$ Hz and $f_{\text{c}} = 50$ Hz, respectively, although other sinusoids with different parameters have been successfully tested. The output signal V_{out} is the voltage across the resistor R_{out}. The WD structure corresponding to the circuit in Fig. 7 is shown in Fig. 8. The 13-port WD junction in Fig. 8 is characterized by a scattering matrix $\mathbf{S}$ which can be computed using equation (4) and setting $\mathbf{Q} = [\mathbf{F}, \mathbf{I}]$, where $\mathbf{I}$ is the 4×4 identity matrix and matrix $\mathbf{F}$ is defined as

$$\mathbf{F} = \begin{bmatrix} 0.5 & 0.5 & -0.5 & -0.5 & 1 & 0 & 1 & 0 & 0 \\ 1 & -1 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ -0.5 & 0.5 & 0.5 & -0.5 & 0 & 1 & 0 & 1 & 0 \\ 1 & -1 & 1 & -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} .$$

In a first implementation, WD models of capacitors and inductors employ the traditional trapezoidal discretization method

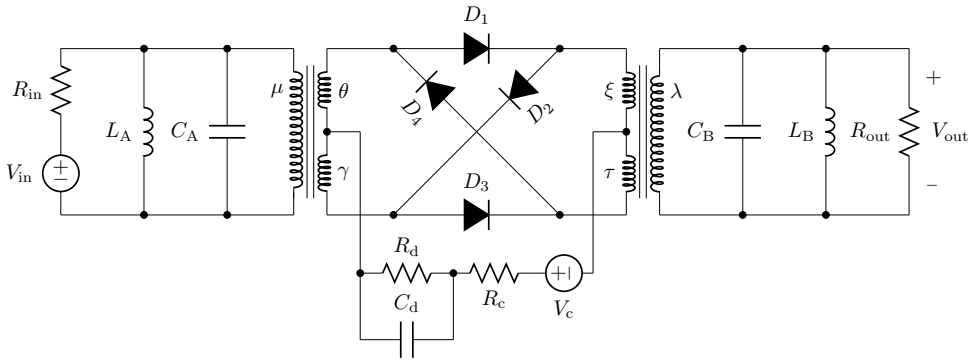


Fig. 7. Dynamic ring modulator circuit.

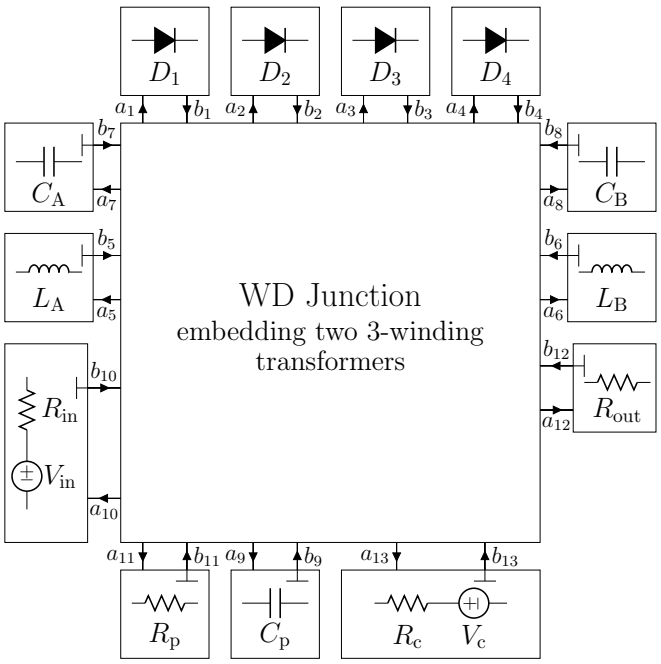


Fig. 8. WD structure corresponding to the circuit in Fig. 7.

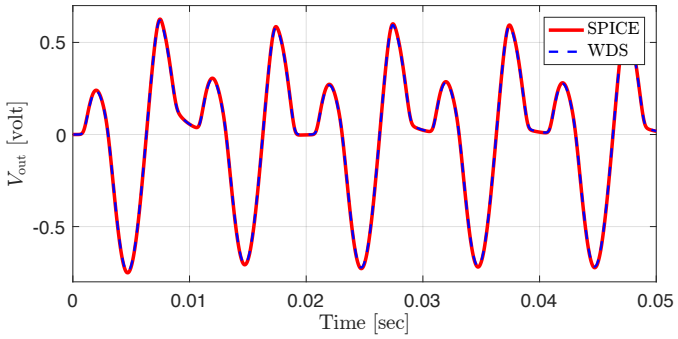


Fig. 9. WD implementation based on SIM employing trapezoidal discretization method with fixed step-size vs LTspice implementation.

with fixed step-size and the sampling frequency is $F_s = 41$ kHz. Fig. 9 shows the high matching between the output signal V_{out} obtained by the WD implementation based on SIM and the same signal obtained by a LTspice software implementation.

In order to test whether a LMSDM of higher order could provide better results in terms of accuracy, we performed a comparison between the already tested WD implementation employing the trapezoidal method and another WD implementation employing BDF 3, i.e., scattering relations (42) and (43) with $M = 3$. In both implementations a fixed step-size is used and the sampling frequency is $F_s = 41$ kHz. A ground truth is obtained linearly interpolating the output samples of a WD implementation employing the trapezoidal method and sampling frequency $F_{GT} = 512$ kHz. Two errors are computed subtracting the ground truth to the output signals V_{out} of the compared WD implementations. These two errors are plotted in Fig. 10; the red line with asterisks indicates the error obtained with the trapezoidal method, while the blue line with circles indicates the error obtained with BDF 3. Fig. 10 shows that the error is generally smaller in amplitude when BDF 3 is used. In particular, the MSE referred to the 0.05 seconds of simulation in the trapezoidal case is 1.34×10^{-10}, while in the BDF 3 case it is 7.28×10^{-11}.

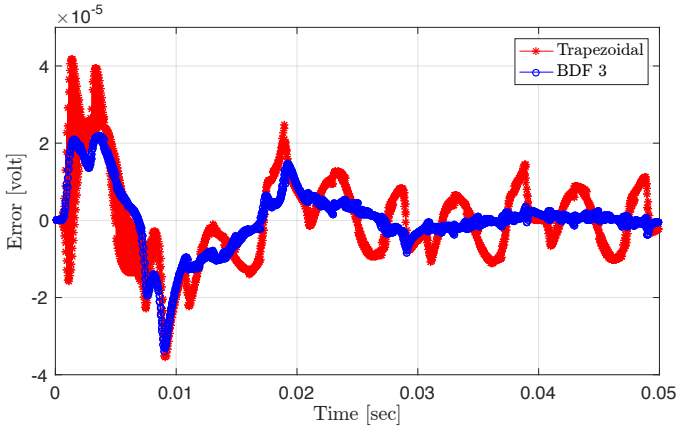


Fig. 10. Comparison between WD implementations of the ring modulator based on SIM employing trapezoidal method and BDF 3, both with fixed step-size. The two curves represent the errors of V_{out} signals w.r.t. the ground truth. The red line with asterisks refers to the trapezoidal method. The blue line with circles refers to BDF 3.

A WD implementation of the dynamic ring modulator circuit using BDF 3 with variable step-size is tested in the last experiment. An initial step-size $h_s = 1/(2F_s)$ with $F_s = 41$ kHz is set. The step-size is then gradually increased up to five times with respect to the initial value as shown in Fig. 11(a).

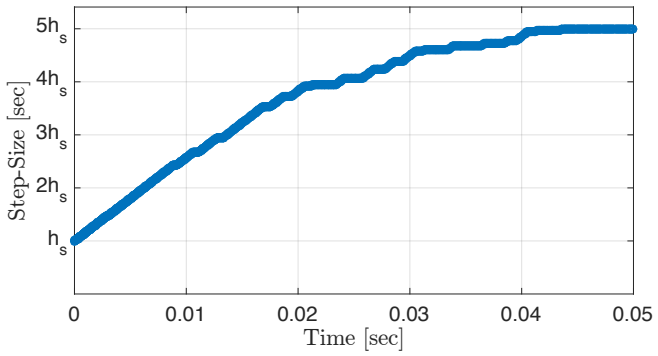
The obtained V_{out} signal is represented by the black line with circles shown in Fig. 11(b) along with the ground truth (green line) also used in the previous experiment. The corresponding error, computed subtracting the ground truth to the output signal V_{out} of the WD implementation based on BDF 3 with variable step-size, is shown in Fig. 11(c). Let us now make a comparison between the V_{out} signal in the variable step-size case and the same signal in the fixed step-size case presented in the previous experiment. As far as the MSE with respect to the ground truth in the first 0.05 seconds of the simulation is concerned, we get 5.48×10^{-11} in the variable step-size case versus the already computed MSE in the fixed step-size case, i.e, 7.28×10^{-11}. Therefore, we get a comparable MSE in the two cases, while reducing the number of samples in the variable step-size case. In fact, the number of samples employed for the first 0.05 seconds of the simulation is 1286 samples in the variable step-size case, versus 2048 in the fixed step-size case.

VII. Discussion, Conclusions and Future Work

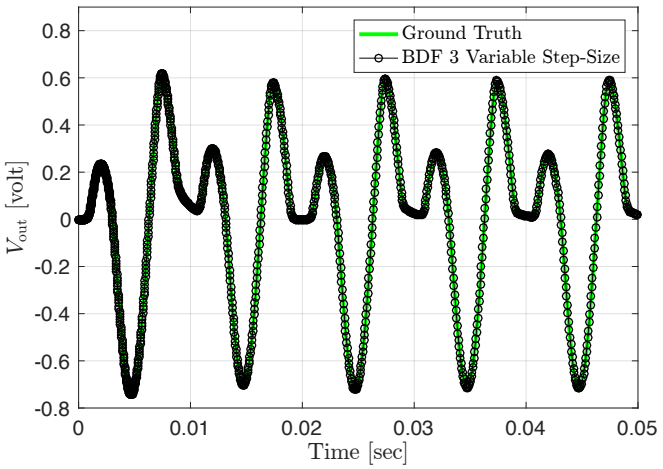
In this article, we presented general WD models of capacitors and inductors based on LMSDMs with variable step-size along with their general adaptation conditions. We showed that the use of LMSDMs alternative to the trapezoidal method with fixed step-size could be advantageous in various situations. The results that we presented pave the way towards the modeling of nonlinear WD structures characterized by adaptive discretization methods that change automatically according to the properties of the processed signals. In this regard, it is important to mention the fact that, when dealing with discretization methods based on variable step-size, some operations on the input and output signals of the WD structure are required for making the implementation compatible with traditional digital audio processing tools based on fixed sampling step. In fact, an interpolation of the samples of the input signals should be performed, so that an eventually non-uniform resampling operation can be executed. Similarly, the non-uniformly spaced samples of the output signals should be interpolated, so that a resampling operation at a fixed rate can be performed.

Moreover, in this article, we showed how the WD fixed-point method SIM, that we recently developed for efficiently implementing circuits with multiple one-port nonlinearities, can be extended to accommodate dynamic nonlinear circuits using the proposed general WD models of dynamic elements. SIM, therefore, proves promising for Virtual Analog modeling of increasingly complex circuits. Future research will be devoted to the application of SIM to dynamic active circuits with multiple multi-port nonlinearities. Recent developments in the convergence analysis of nonlinear delay-free loop filter networks [63], [64], in fact, could help us find new theoretical tools for studying the convergence of SIM applied to a broader class of circuits than the one considered in [8], [39] and in this article.

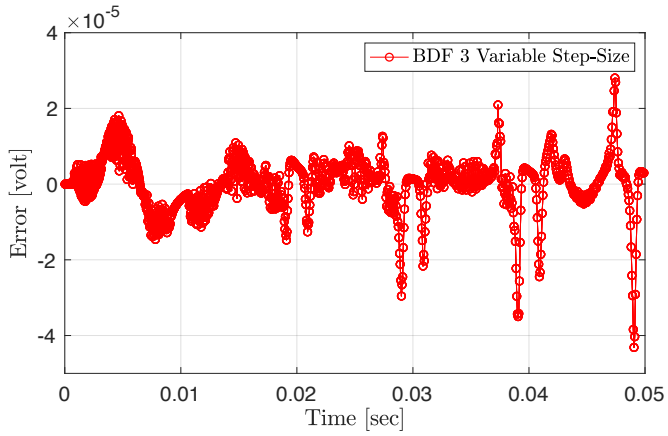
More generally, we showed how capacitors and inductors can be implemented like time-varying resistive voltage (or current) sources in the WD domain. It follows that the proposed WD models of dynamic elements can be readily used in



(a)



(b)



(c)

Fig. 11. WD implementation of the ring modulator based on SIM employing BDF 3 with variable step-size. Fig. 11(a) shows the variation in time of the step-size $h[k]$. Fig. 11(b) shows V_{out} signals; the green line refers to the ground truth, while the black line with circles refers to the WD implementation employing BDF 3 with variable step-size. Fig. 11(c) shows the error of V_{out} signal w.r.t. the ground truth.

conjunction with existing methods alternative to SIM for the WD implementation of circuits with multiple nonlinearities [27], [29], [38].

The proposed approach for the WD modeling of dynamic elements could also be applied for generalizing the WD models of time-varying reactances discussed in [65] to a larger class of discretization methods.

Despite voltage waves considered in this article are the most widespread in the literature on WDFs, WD structures based on alternative types of waves, such as those characterized by different units of measure [48], [57]–[59] or two free parameters per port instead of one [36], [57], have recently proved to possess peculiar interesting properties. WD models of dynamic elements based on LMSDMs and generalized definitions of waves, including the most used as particular cases, can be straightforwardly derived combining the modeling approach used in recent publications [48], [57], [58], [65] to the results presented in this manuscript.

Finally, a systematic study on the accuracy and stability properties of specific LMSDMs with variable step-size in WD structures is postponed to future research.

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