Multi-port dynamic compact thermal models of dual-chip package using model order reduction and metaheuristic optimization

Brice Rogié[a,b], Lorenzo Codecasa[c], Eric Monier-Vinard[b,*], Valentin Bissuel[b], Najib Laraqi[a], Olivier Daniel[b], Dario D'Amore[c], Alessandro Magnani[d], Vincenzo d'Alessandro[d], Niccolò Rinaldi[d]

[a] Université Paris Ouest, Laboratoire Thermique Interfaces Environnement, 50 rue de Sèvres, 92410 Ville d'Avray, France
[b] Thales Global Services, 19-21 Avenue Morane Saulnier, Vélizy-Villacoublay, France
[c] Department of Electronics, Information and Bioengineering, Politecnico di Milano, Milan, Italy
[d] Department of Electrical Engineering and Information Technology, University Federico II, Naples, Italy

ABSTRACT

Delphi-like boundary condition independent (BCI) compact thermal models (CTMs) are the standard for modelling single die packages. However their extraction, particularly in the transient case, will be time consuming due to complex numerical simulations for a large number of external conditions. Lately, new approaches to extract a BCI dynamical CTM (DCTM), based on model order reduction (MOR) were developed. Despite the numerous advantages of this recent method, the lack of numerical tools to integrate reduced-order models (ROM) makes it difficult to use at board level. In this study, a novel process flow for extracting Delphi-inspired BCI DCTMs is proposed. Thus a detailed three-dimensional model is replaced by a BCI-ROM model using FANTASTIC matrix reduction code to generate the data used in the creation of a Delphi-style BCI DCTM. That hybrid reduction method has been applied, at first on a single-chip package (QFN16) then on a dual-chip package (DFN12). Their derived CTM and DCTM have been compared in term of accuracy and creation time using, or not, MOR reduction technique. The results show that for a similar accuracy, the integration of MOR technique allows minimizing the time-consuming numerical simulations and consequently reduce the thermal network creation time by 80%.

1. Introduction

The thermal aspect of electronic devices, especially packages of active semi-conductors, has always been an issue for electronic designers. The widely used standard thermal parameter, called Junction-to-Ambient Resistance, fails to accurately predict the heat path from the chip to the exterior of its package and so to its surroundings.

The thermal characterization of multi-chip packages became a major issue. Indeed, this one cannot be anymore based on the usual single-resistor thermal metrics. Commonly, the specific behaviour of the chip is defined by a metric known as the junction-to-ambient thermal resistance or by the acronym RJA. Its definition is given by a JEDEC standard called JESD51-2A [1].

$$R_{JA} = (T_J - T_A)/Q \tag{1}$$

Its value indicates the sinking capacity of the total heating power (Q) of the device through all the thermal paths between chip junction (T_J) and ambient air (T_A). The junction temperature (T_J) has a huge impact on electronic performances and on reliability. The way of how the junction temperature accelerates the ageing of a device can be estimated using Arrhenius equation.

A failure criterion can be calculated which compares the normal-use operating temperature to a critical-use temperature condition. This one is defined as "Accelerating temperature Factor", its definition is given by the JEDEC standard JESD74A [2].

$$AF_T = exp\left[\frac{Ea}{k_B}\bullet\left(\frac{1}{T_j^n} - \frac{1}{T_j^m}\right)\right] \tag{2}$$

where

- Ea is the Energy of activation that is, for instance, 0.7 eV for bipolar Integrate circuit,
- K_B is the Boltzman constant ($8.617 \cdot 10^{-5}\,eV{\cdot}K^{-1}$),
- T_j^n is the junction temperature (in K) at normal use condition, and
- T_j^m is the junction temperature (in K) at modified use condition.

It can be shown that every 10 °C reduction results in a doubling

* Corresponding author at: Université Paris Ouest, Laboratoire Thermique Interfaces Environnement, 50 rue de Sèvres, 92410 Ville d'Avray, France.
E-mail address: eric.monier-vinard@thalesgroup.com (E. Monier-Vinard).

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lifetime, or at the opposite, in accelerated failure occurrence.

In multi-chip packages, the thermal constraints of each chip are depending of their location (stacked, side by side) as well as the close proximity of the others active parts. Consequently, the prediction of the component sensitive temperatures based on a single junction-ambient resistance can be quite wrong. Indeed, the heat dissipation of each chip may vary depending on the operating conditions and it is hard to determine who will be the hottest one.

It occurs that the use of multi-source thermal resistances is henceforth mandatory to represent multi-die package. A theoretical approach using linear superposition principle has been proposed by some authors. But this one requires being capable to sense simultaneously the temperatures of all embedded active chips, a major difficulty on real device. Moreover, the definition of the multi-source thermal network will only address a single heat path, from the chip junctions to a cooled board structure, which strongly limits is practical usability.

On the other hand, the numerical modelling of a fine three-dimensional representation of complex multiple heating sources package is today easier as well as Printed Circuit Board on which it is mounted [3]. That accurate modelling allows a new way to calibrate the thermal behaviour of a component from experiment and then derive an appropriate thermal network.

In order to improve the reliability of the thermal prediction of electronic equipment, a procedure to extract relevant multi-path thermal model is described in the current study.

The use of relevant detailed thermal models (DTM), which are a fine representation of the complex geometry of the die package, is limited by computation resources. The numerical model of a package generally requires hundred thousands of nodes in thermo-fluidic simulation software. A board-level thermal analysis, with thousands of electronic components including the complex board's geometry, will be excessive if each component is modeled using DTMs.

To overcome the computing limitation, Black-Box models of electronic packages have been developed. Those surrogate models have the benefits of correctly predicting the thermal path of the packages, within a good tolerance, without the need for a full geometry description.

2. Concurrent model reduction approaches

Several approaches have been investigated to provide “Black-Box” thermal models of single chip packages from numerical simulation [4]. The most accomplished concept is the Compact Thermal Model (CTM) established by the Delphi Consortium in 1996. This one has been standardized by the JEDEC community, as JESD15-4 guideline [5].

A CTM is an abstraction of a component thermal behaviour based on detailed component modelling and experiment test results. To build a CTM model, Delphi's approach promotes the use of a thermal resistances network which links the sub-divided exterior surfaces of the component to a sensitive node, called junction. A condensed overview of the Delphi's method and JEDEC standardization aspects has been written by Lasance [6]. However, the practical application of Delphi's method requires choosing a suitable optimisation scheme, a non-trivial task to non-experts.

The feasibility of applying a stochastic search algorithms was studied to derive a steady-state CTM by several authors [7–9], which demonstrate the high capabilities of Genetic Algorithms for optimization.

The latter has been exercised, with success, on several electronic packaging cases [10].

Unfortunately, Delphi's method focused only on the creation of steady-state one-source thermal network and the generation of Dynamical Compact Thermal Model (DCTM) remains a problematic [11]. To resolve that issue, some studies were done [12] [13] and then an in-house procedure established.

3. Delphi's method constraints

If Delphi's project started the movement to define a standardized guidance [5] to build Boundary-Condition-Independent (BCI) surrogate thermal model of electronic component, it attractiveness diminished due to its limited spectrum of application.

The main drawbacks of the method are highlighted below:

- allow only a small number of heat sources [14],
- approximate only a small number of temperatures and heat fluxes of the detailed thermal model,
- need quite large training and test sets [6, 14],
- require quite large sets of time-consuming transient thermal simulations of the detailed model [15],

Moreover, the BCI-DCTM accuracy cannot be chosen. This latter strongly depends on a smart selection of “Black-box” settlement details to approximate the DTM behavior.

4. New alternative approaches

In order to extend Delphi's scope, other reduction approaches, such as model order reduction (MOR), are now available. These recent methodologies [16] are based on matrix reduction algorithms, introduced in the early eighties [17], and was developed for systems and control theory.

For electronic device modeling, the proposed approaches for constructing DCTM are done with fixed or at most parametric boundary conditions [18, 19].

Only few works have been proposed for the construction of boundary-condition-independent DCTMs [20, 21]. These works use proper orthogonal decomposition (POD) method, which was developed for computational fluid dynamics and requires large set of time-consuming transient thermal simulations of the detailed model.

In this paper, a multipoint moment-matching (MPMM) approach is exploited with analytically determined expansion frequencies that is structure-preserving as well as extremely computational efficient, as highlighted in [22].

5. Study purpose

Based on these two visions for minimizing computational resources, a hybrid reduction method is promoted that suggests the integration of a reduced matrix model to calculate a set of Boundary Conditions, instead of a detailed model. By ensuring a low discrepancy between the detailed model and the ROM model, the time to build a DCTM can be drastically shortened as demonstrated in [15].

6. Compact thermal models of electronic device

Two main reduced thermal models technics are summarized in this section: The standard compact thermal model [5] and the Reduced-Order Model [17].

6.1. Dynamical compact thermal models

The conventional black-box CTMs or DCTMs are built on results extracted from numerical simulations using a metaheuristic optimisation based on genetic algorithm (GA).

For CTMs generation, the Delphi's method has been revised to enhance its relevance and effectiveness. The added steps are discussed in [10, 14, 23]. As mentioned, the steps for the identification of the thermal capacities are given in [12, 13].

Fig. 1 summarizes the flow chart describing the ordered steps follow to develop our in-house RC network.

At first, the thermal resistances values are fitted using a custom

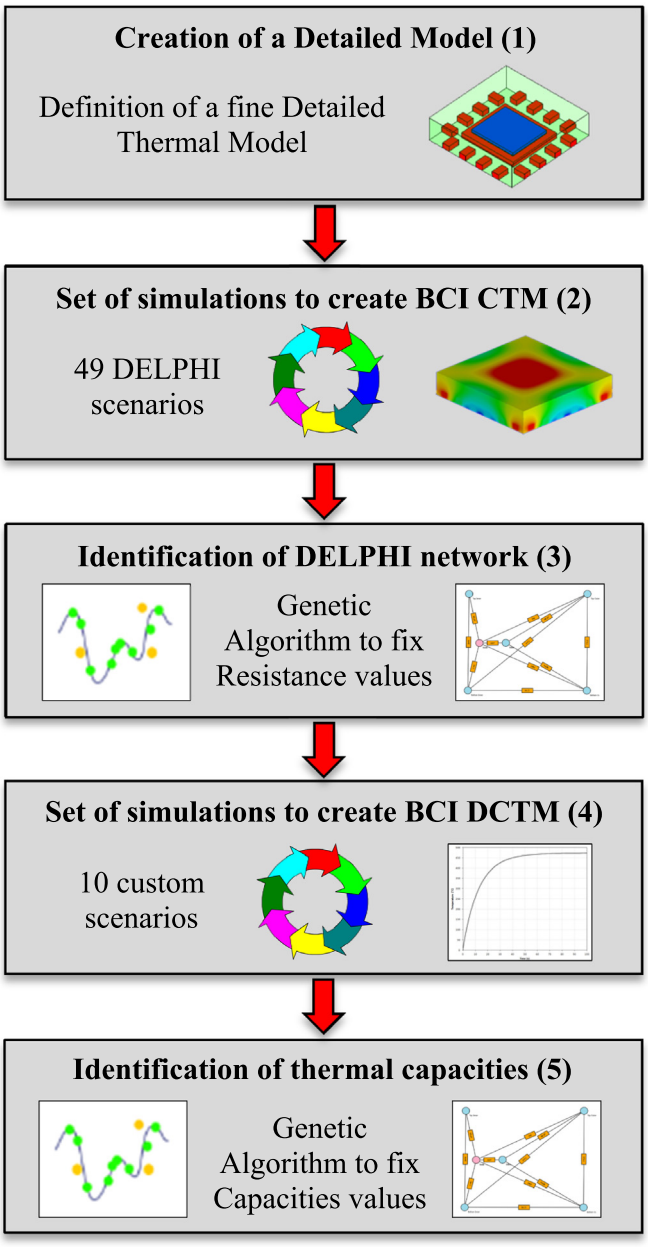


Fig. 1. Creation flow of BCI DCTM using multi-objective Genetic Algorithm (GA) optimization.

objective function (3). Its form is expressed as a weighted-sum equation:

$$F(\theta, Q) = \omega \bullet f(\theta) + (1 - \omega) \bullet f(Q) \tag{3}$$

The function $f(\theta)$ accounts the discrepancies of the average temperature of every external surfaces as well as the maximum temperature of inner nodes as called junction. $f(Q)$ sums up the discrepancies of the heat flux passing through the external surfaces [10]. The resulting function $F(\theta,Q)$ is the GA fitness score with 1 as optimum. Moreover, the model suitability can be controlled from a temperature weight factor, name ω. To improve the accuracy of the derived CTM, a GA optimization of the node number describing the overall surfaces of the component can be done [14]. Each surface is then subdivided in a set of more appropriate isothermal areas.

For thermal capacities identification, only the temperatures for every time steps are fitted. So, the time-depending objective function (4) accounts the discrepancies of the average temperature of each external surface as well as the maximum junction temperature [13].

$$f_t(\theta) = 1 - \frac{\omega t}{N} \cdot \sum_{b=1}^{N_{BC}} \sum_{n=1}^{N_N} \sum_{k=1}^{N_{TS}} [\, \Delta\theta_{n=j,b}(t_k)\,]^2 - \frac{1-\omega t}{N \cdot (N_N - 1)} \cdot \sum_{b=1}^{N_{BC}} \sum_{n=1}^{N_N} \sum_{k=1}^{N_{TS}} [\, \Delta\theta_{n\neq j,b}(t_k)\,]^2$$

$$\text{With} \quad N = N_N \cdot N_{BC} \cdot N_{TS} \tag{4}$$

N_{BC} corresponds to the number of boundary conditions, N_N the number of nodes, N_{TS} the number of time steps and t_k the current time at the step k.

As previously, a weight parameter, named ωt, balances the accuracy for all nodal temperatures. The consideration of the external temperatures allows minimizing heat flux discrepancies.

Further, the predictions of DCTMs can be improved using a GA procedure dedicated to implement new internal nodes.

6.2. Model order reduction by FANTASTIC code

The FANTASTIC (FAst Novel Thermal Analysis Simulation Tool for Integrated Circuits acronym) code is a matrix reduction approach for creating reduced-order models. The ROM model can be either used for steady-state or transient analysis. The extraction procedure is given in [24, 25].

The input of the FANTASTIC model is composed of the numerical mesh of one component's geometry as well as the definition of its material properties, the boundary conditions and the heat sources localisation. All these information can be found in the mass matrix M and the stiffness matrix K of the detailed model extracted from COMSOL®. The discretized heat diffusion problem is then defined as:

$$M \bullet \frac{\partial x(t)}{\partial t} + K \bullet x(t) = G \bullet P(t) \tag{5}$$

With G the [N × n] matrix of port power density distribution, $P(t)$ the n-row vector of port powers and $x(t)$ being the N-row temperature rise distribution vector. Finally, the n-row column vector $T(t)$ collecting the temperature is written as:

$$T(t) = T_0 + G^T \bullet x(t) \tag{6}$$

Eq. (5) is not directly solved. Instead a ROM model is built using an extended version of the MPMM algorithm [26]. The resulting BCI reduced model is similar to Eqs. (5) and (6):

$$\widehat{M} \bullet \frac{\partial \hat{x}(t)}{\partial t} + \widehat{K} \bullet \hat{x}(t) = \widehat{G} \bullet P(t) \tag{7}$$

The temperature distribution with the initial temperature T_0:

$$T(t) = T_0 + \widehat{G}^T \bullet \hat{x}(t) \tag{8}$$

The reduced matrices $\widehat{M}$, $\widehat{K}$ and $\widehat{G}$ are defined using the transfer matrix V [N × k] (with $k \ll n$), initially found by the use of the MPMM algorithm [26].

$$\widehat{M} = V^T \bullet M \bullet V \tag{9}$$

$$\widehat{K} = V^T \bullet K \bullet V \tag{10}$$

$$\widehat{G} = V^T \bullet G \bullet V \tag{11}$$

Finally the temperature rise distribution vector is found by the following equation:

$$x(t) = V \bullet \hat{x}(t) \tag{12}$$

The results of the ROM model are assured to be lower than the desired relative error ε, as described in [24]. The eigenvalue problem, in Eq. (7) is then solved for a reduced number of Degree of Freedom (DoF) which lowers considerably the computation time.

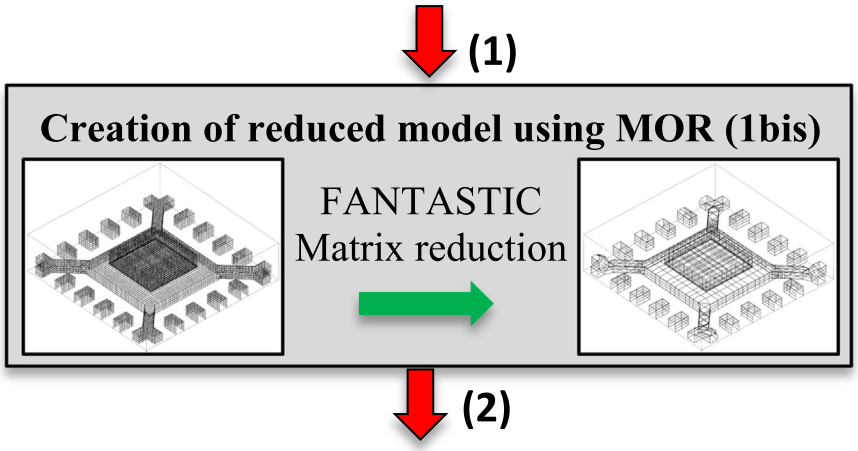


Fig. 2. FANTASTIC matrix reduction algorithm applied to the DTM in the creation flow of a DELPHY-style DCTM.

7. Hybrid DCTM creation using MOR technique

More than ever, the thermal modelling of complex 3D-packaging with non-conventional dies placement as well as numerous number of metallic wire connections, needs large computation resources. Consequently, the numerical simulation of DELPHI's 49 scenarios is going to be a major time-consuming task. Furthermore, that computation time will significantly increase when transient simulations are mandatory.

Thus the capability to replace the numerical computation of a detailed model by a must faster mathematical Reduced-Order Model appears very attractive if the thermal behaviour of the original model is properly matched.

Therefore the creation flow, seen in Fig. 1, was modified [15] to insert an additional step using the FANTASTIC solver, which derives a ROM model, as pictured Fig. 2.

At the opposite of metaheuristic optimization, the appliance of the deducted ROM model is pre-established. In the studied case, the temperatures and the heat fluxes leaving the external surfaces are assured to be within 0.1% difference with the numerical detailed model, for a heat transfer coefficient range from 1 to 10^9 $W{\cdot}m^{-2}{\cdot}K^{-1}$. Given the high agreement of that reduced-order model, this one enables to carry out all the mathematical calculations for the identification of CTM and DCTM parameters.

To illustrate the relevance of that creation procedure, a thermal compact model of an industrial package has been performed using both the Delphi-inspired procedure and the new proposed method. The results have been compared in terms of accuracy and creation time.

8. Test case 1: single-chip QFN16

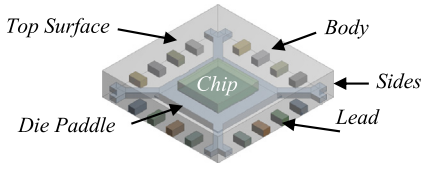
The industrial package under investigation is a well-known QFN16 (Quad Flat No Leads). This single-chip package has the particularity of being soldered to the electronic board by 16 in-built leads, as well as its die paddle, which are located on its lower surface. The definition of the package is reported in Table 1.

The chip dissipation is located on its upper surface and its material properties are considered independent of the temperature variation (linear heat diffusion problem).

The detailed numerical model of the QFN16 was created using Finite Element Method (FEM) software. The final mesh, after meshing influence study, is composed of 170 k elements. The temperatures extracted from the reduced-order model were computed using mathematical software.

From the QFN16 fine detailed model, two DCTMs were created from:

Table 1
QFN16 geometry and material properties.



Material	k @ 25 °C ($W{\cdot}m^{-1}{\cdot}K^{-1}$)	L (mm)	W (mm)	H (mm)
Chip	150	1.4	1.4	0.25
Glue	2.1	1.4	1.4	0.03
Die-pad	260	2.2	2.2	0.2
Lead (×16)	260	0.23	0.4	0.2
Body	0.66	4	4	0.8

- Delphi-inspired heuristic-procedure, named D-DCTM,
- Hybrid-method using MOR model, defined as H-DCTM.

Then these two DCTMs were compared in term of precision, or score, and creation time for the steady-state (CTM) and transient (DCTM) cases.

The numerical calculations were performed on 4 cores of an Intel Xeon E5–2650 and an Intel i7 for the ROM extraction.

8.1. Compact thermal model for steady-state

In this section, only the creation of a conventional DELPHI steady-state compact model is discussed.

The 49-set boundary conditions applied to the package are meant to reflect all the conditions that a component encounters in typical electronic applications. The values of the heat transfer coefficients vary from 1 to 10^9 $W.m^{-2}.K^{-1}$, and are listed in [23].

These BC are submitted to both the numerical solver (D-CTM) and the reduced-order model (H-CTM). For both models, the CTM is composed of:

- One inner node as called junction,
- Two top nodes: Top inner (the projected chip's area on top surface) and Top outer (the remaining surface),
- Two bottom nodes: Bot inner (the projected die-pad's area on lower surface) and Bot outer (the remaining surface),
- One Sides node (the 4 regrouped lateral edges),
- One Leads node (the 4 regrouped leads areas).

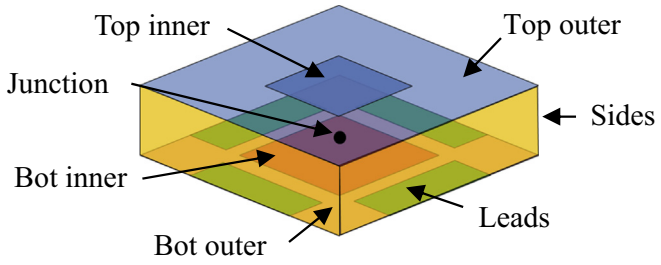


Fig. 3. CTM representation of 7 nodes QFN16.

Table 2
Score of Delphi-inspired and Hybrid CTMs.

	D-CTM	H-CTM
Score	0.99	0.99
ΔT (%)	0.3	0.4
Δφ (%)	< 0.1	< 0.1

The representation of the CTM is provided in Fig. 3, where the CTM's outputs are specified.

The resulting steady-state score of the two CTMs are listed in Table 2, as well as the average temperature (ΔT) and heat flux differences (Δφ) for all nodes compared with the DTM.

The GA being a metaheuristic algorithm, the results are, by definition, not reproducible. Thus, the score of the CTM is the best value obtained after 20 Genetic Algorithm trials.

In terms of creation time, the total duration was categorized in function of the different steps of the flow chart:

- Step1: The meshing of the QFN16,
- Step 1bis: The pre-reduction of the QFN16 using FANTASTIC Multi Order Reduction software (H-CTM),
- Step 2: The simulations of the 49 BC using a numerical software (D-CTM), and
- Step 3: The fitting of the resistor values of the steady-state thermal network using our Genetic Algorithm (GA).

The duration time for each step is summarized below (see Fig. 4 and Table 3):

As highlighted in the previous table, the creation time of the CTM is shortened by 60% in comparison with the traditional D-CTM.

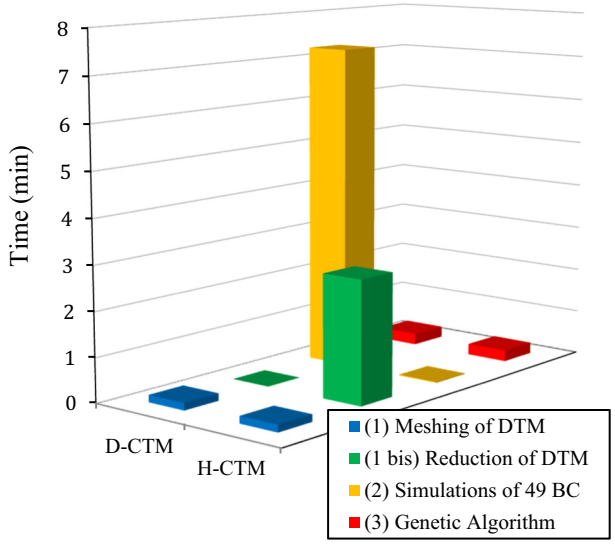


Fig. 4. Distribution of overall CTM creation time.

Table 3
Creation time of Delphi-inspired and Hybrid CTMs.

Step	Time (min)	
	D-CTM	H-CTM
1	0.2	0.2
1bis	Null	2.8
2	7.3	< 0.1
3	0.2	0.2
TOTAL	7.7	3.2

This benefit is mainly achieved by switching from numerical computation (which represents 95% of the total time) to a lower order matrix calculation using a reduced-order model.

The time required by the GA to converge (step 3) is defined by the following formulae:

$$t_{GA}(F_\infty) = t\left(0.99 \bullet \max_{i=1\ to\ N} F_i(\theta, Q)\right) \tag{13}$$

A set of thermal networks is created using the GA. The final time (t_{GA}) is found when the GA reaches a score corresponding to 99% of the maximum score obtained after the 20 trials. The GA optimization provides high score in few seconds but takes a significant time to reach its final value. It is important to define a stoping criteria to avoid unecessary time waste. Fig. 5 represents the variation of the average score after 20 trials in function of the calculation time.

The average score only increases by 1% from 15 s to 5 min. The GA proves its ability to reach rapidly its suitable score in the network's Resistance search.

Furthermore, the convergence speed of the GA mainly depends on the number of unknowns.

In the case of the construction of a Resistance network, the total number of unknowns is equal to $N \cdot (N-1)/2$ with N the number of nodes. The 7 nodes QFN16's CTM has 21 unknowns.

The next section focuses on last steps of the creation flow of a DCTM, corresponding to the final RC network building.

8.2. *Dynamic compact thermal model*

The next step of a DCTM creation process flow is the identification of the thermal capacities values. Complementary transient simulations have to be performed to provide reference data. The number of Boundary Conditions for the transient simulation is limited to 10 (listed in the appendix).

As for the steady-state case, the score of both DCTMs and the temperature divergence with the detailed simulations are reported in Table 4. The temperature divergence is based on the normalized root mean square error (NRMSE) which is given in Eq. (14).

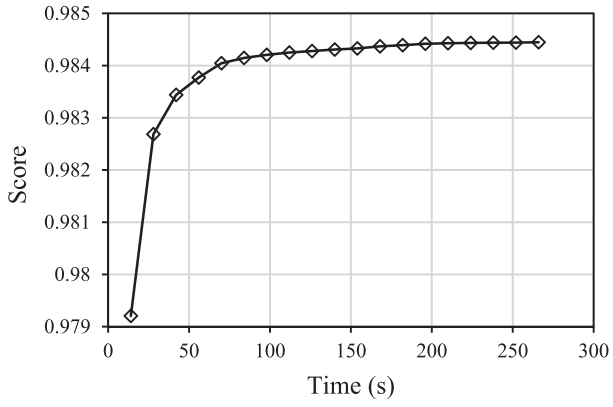


Fig. 5. Evolution of CTM score in function of time.

Table 4
Score of Delphi-inspired and Hybrid DCTMs.

	D-DCTM	H-DCTM
Score	0.997	0.997
ΔT (%)	0.9	1.0

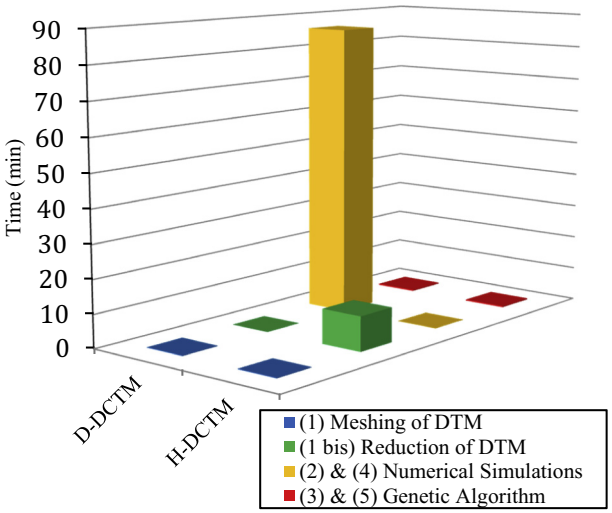


Fig. 6. Distribution of overall DCTM creation time.

$$NRMSE = \sqrt{\frac{\sum_{n=1}^{N}(x_n - y_n)^2}{N}} / (x_{max} - x_{min}) \quad (14)$$

The temperature difference is computed at each time step and then normalized by the maximum temperature. N corresponds to the number of time steps in the transient simulations.

The score as well as the average temperature difference are similar for both DCTM methodologies. The low discrepancy between the detailed model and the reduced models allows achieving equivalent compact models.

As for the steady-state analysis, the overall time for creating a DCTM is shown in Fig. 6 with the four principal steps. Nonetheless, several steps have been grouped due to their similarities:

- The time taken by the numerical simulations for the steady-state and transient cases is merged: step 2 & 4,
- The time taken by the GA to adjust the thermal resistance values and the thermal capacities: step 3 & 5.

The time required for the GA to build a capacity network follows Eq. (13) as for the resistance network creation (Table 5).

The DCTM creation time, including both steady-state and transient simulations is shown in the next table.

First of all, the reduction of the detailed model takes more time than for CTMs due to the added transient term in the heat equation.

Table 5
Creation time of Delphi-inspired and Hybrid DCTMs.

Step	Time (min)	
	D-DCTM	H-DCTM
1	0.2	0.2
1bis	Null	10.3
2 & 4	86.3	< 0.1
3 & 5	*0.3*	*0.3*
Total	86.8	10.8

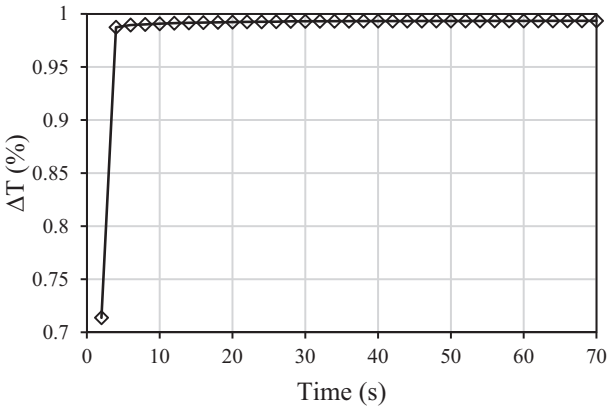


Fig. 7. Evolution of DCTM score in function of time.

However, the GA takes significantly less time to converge because of fewer unknowns. The number of unknowns corresponds to the number of nodes (one thermal capacity per node), 7 for the QFN16's CTM, three times less than for the resistance's network search.

This explains the reduction in time of the GA's convergence, as seen in Fig. 7.

Combining a significant drop in simulation time, as well as a fast GA convergence, the DCTM creation time is reduced by 87%.

Furthermore, the conversion of the ROM in a RC network (or classical DCTM) takes < 4% of the total duration time, and is therefore insignificant.

To ensure the feasibility of the investigated new reduction approach, the same creation procedure has been applied to a similar package where the die's connectors are modeled.

9. Test case 2: industrial single-chip QFN16

The QFN16 has been completed to better represent the realistic design of an actual electronic component.

More sensitive details such as the gold wire connections linking the active part of the chip to the leads where added. The real geometry of the package is shown on Fig. 8 as well as its numerical model.

The addition of electrical connexions adds complexity in the model's meshing. From an initial meshing of 170 k elements, the new one is composed of > 1.7 M elements thus having a great impact on the calculation time. The creation time of every steps of the DCTM is shown in the next table (Table 6).

The score and the average temperature predictions of the new QFN16 are shown in the next table (Table 7).

The reduction in time is similar to the first case, around 80%. The use of a ROM model allows creating a DCTM model of a realistic package in less than 1 h while keeping a high accuracy level.

The last test case is the main objective of the studied about the creation of a dual-chip electronic package. The objective is to provide a multi-path RC network capable to predict the influence of several buried heating sources on the sensitive elements of multi-chip component.

10. Test case 3: industrial multi-chip the DFN12

The studied DFN12 is an industrial dual-chip package. Two dies are mounted on its die-pad, which joins the chip to the bottom surface of the package. As for the industrial QFN16, wire gold-bondings link the two chips to the lateral leads.

A three-dimensional representation of the DFN12 and its constitutive material are displayed Table 8.

The mesh of the dual-chip package is composed of 715 k tetrahedral elements. The reduction of the DFN12 takes 25 min.

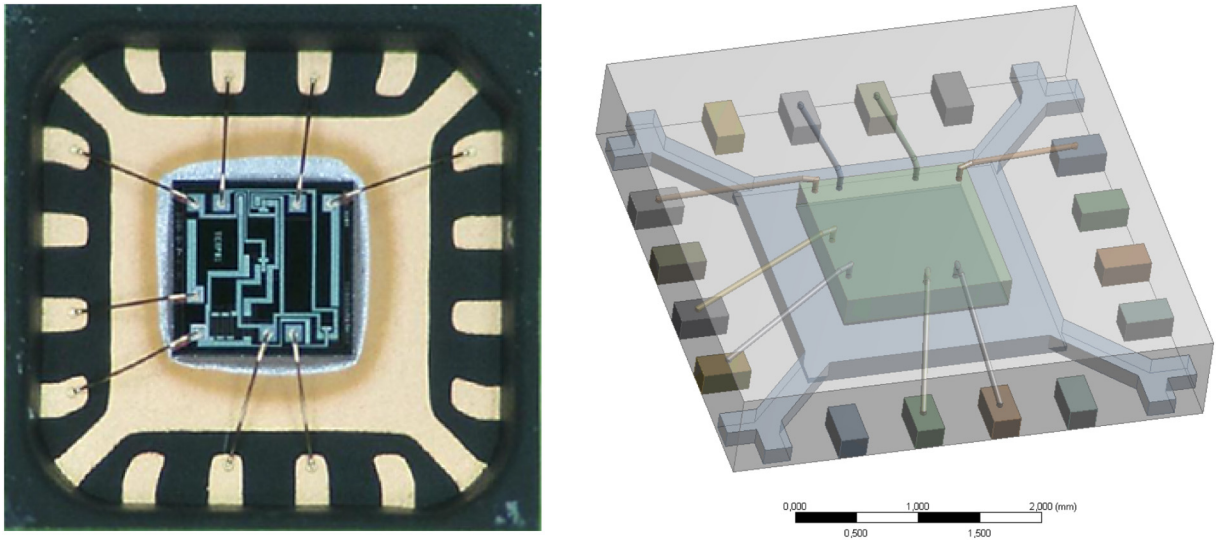


Fig. 8. Internal view (left) and 3D geometry (right) of the QFN16 with gold wire connections.

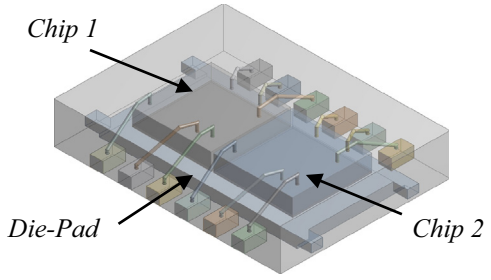
Table 6
Creation time of Delphi-inspired and hybrid DCTMs.

Step	Time (min)	
	D-DCTM	H-DCTM
1	1.1	1.1
1bis	Null	36
2 & 4	193.5	< 0.1
3 & 5	*0.3*	*0.3*
Total	194.9	37.4

Table 7
Score of QFN16's DELPHI inspired and Hybrid DCTMs.

	D-DCTM	H-DCTM
Score	0.997	0.997
ΔT (%)	2.2	2.3

Table 8
DFN12 geometry and material properties.



Material	k @ 25 °C ($W{\cdot}m^{-1}{\cdot}K^{-1}$)	L (mm)	W (mm)	H (mm)
Chip (×2)	150	1.4	1.4	0.25
Glue (×2)	2.1	1.4	1.4	0.03
Die-pad	260	3.5	1.9	0.2
Lead (×12)	260	0.23	0.4	0.2
Body	0.66	4	3	0.7

The compact model of the DNF12 is composed of 9 nodes:

- Two inner nodes, considering each chip junction,
- Two Top inner (projection of chip 1 and chip 2 on top's surface),
- One Top outer (remaining top surface),
- Two bottom nodes: Bot inner (the projected die-pad's area on bottom surface) and Bot outer (remaining bot surface),
- One Sides node (the 4 regrouped lateral edges), and
- One Leads node (the 2 regrouped leads areas).

A representation of the DFN12's nodes is pictured Fig. 9.

To build the expected dual-chip compact thermal model, the influence of the mutual heating of each chip has to be taken into account.

Consequently, the 49 steady-state Delphi scenarios and the 10 transient custom scenarios have to be repeated for each die, successively active, then when both are actives.

That requisite procedure leads to a huge computation time in the D-DCTM creation procedure. Obviously, the use of a ROM pre-reduction procedure is then particularly useful to reduce the time to generate scenarios data. The next graph summarizes the creation time of the DFN12's DCTM for both methods (Table 9).

The overall creation time is reduced by > 90%. Thus prohibitive numerical computations are eliminated. Using MOR approach, the generation of scenarios thermal data drop from > 6 h to less than 1 s, without degrading their accuracy.

Finally the score and corresponding accuracy of the DCTMs are summarized (Table 10):

11. Conclusion

The setting up of an hybrid reduction technique where a Reduced-

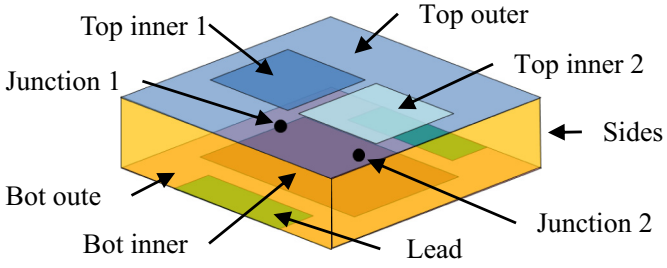


Fig. 9. CTM representation of 9 nodes DFN12.

Table 9
Creation time of Delphi-inspired and Hybrid DCTMs.

Step	Time (min)	
	D-DCTM	H-DCTM
1	0.2	0.2
1bis	Null	25
2 & 4	381.8	< 0.1
3 & 5	10.3	10.3
Total	392.3	35.5

Table 10
Score of DFN12's DELPHI inspired and Hybrid DCTM.

	D-DCTM	H-DCTM
Score	0.988	0.990
ΔT (%) & Δφ (%)	0.6 & 0.5	0.6 & 0.8
Score	0.995	0.991
ΔT (%)	1.7	2

Order Model is used, instead of a detailed model, in the creation process of the Delphi-style compact model appears to be an efficient solution in term of creation time.

A consequent cut of 80% in the overall process time can be achieved without degrading the final score of single port Dynamic Compact Thermal Model. The reduction time is even more enhanced for multi-port DCTM, with a 90% time reduction while keeping a very high accuracy.

The adoption of that extra step in the creation flow of a Delphi-inspired DCTM procedure is particularly relevant for complex geometries with a rather important mesh.

It occurs that the creation time of complex multi-chip packages can be reduced to less than an hour, whatever the number of heating sources, which gives much more flexibility to thermal designers to generate relevant thermal of various electronic components.

Finally, according with Delphi spirit, the few nodes (usually less 10) of the derived multi-chip multi-path RC network allows simulating, with a very good accuracy, the thermal behaviour of populated electronic boards, with thousands of components, in any state-of-the-art software, which is the main study concern.

Appendix A

Custom 10 scenarios for DCTM creation

Scenarios	Heat transfer coefficient ($W \cdot m^{-2} \cdot K^{-1}$)		
	Top	Bot	Sides & Leads
1	15	100	5
2	50	250	15
3	800	20	5
4	0.1	0.1	0.1
5	400	1000	15
6	0.1	100	50
7	1000	40	100
8	100	0.1	5
9	15	200	200
10	30	200	50

- QFN16 **with no bondings**

Thermal resistance network ($K \cdot W^{-1}$) of H-CTM.

	Top in	Top out	bot in	Bot out	Sides	Leads
Junction	1301	174	8	568	–	–
Top in		–	321	–	–	–
Top out			–	325	118	1529
Bot in				95	304	–
Bot out					712	373
Sides						91

Thermal capacities ($mJ \cdot K^{-1}$) of H-CTM.

Junction	Top in	Top out	Bot in	Bot out	Sides	Leads
3.0	0.8	11.2	2.9	2.1	2.3	4.6

- QFN16 **with bondings**

Thermal resistance network ($K{\cdot}W^{-1}$) of H-CTM.

	Top in	Top out	Bot in	Bot out	Sides	Leads
Junction	1291	154	9	660	–	640
Top in		–	249	–	–	–
Top out			–	439	115	758
Bot in				107	480	–
Bot out					340	1398
Sides						121

Thermal capacities ($mJ{\cdot}K^{-1}$) of H-CTM.

Junction	Top in	Top out	Bot in	Bot out	Sides	Leads
4.6	0.3	11.1	2.1	0.9	2.6	5.7

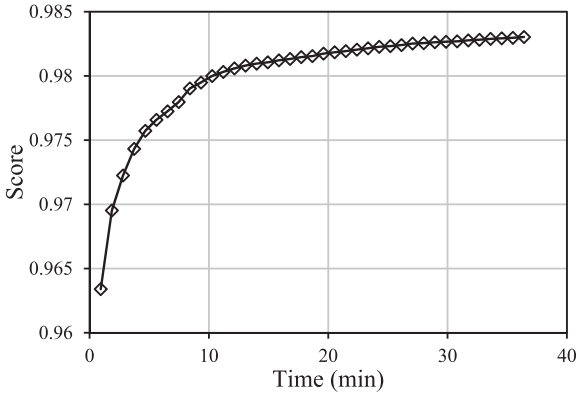
- DFN12 **with bondings**

Thermal resistance network ($K{\cdot}W^{-1}$) of H-CTM.

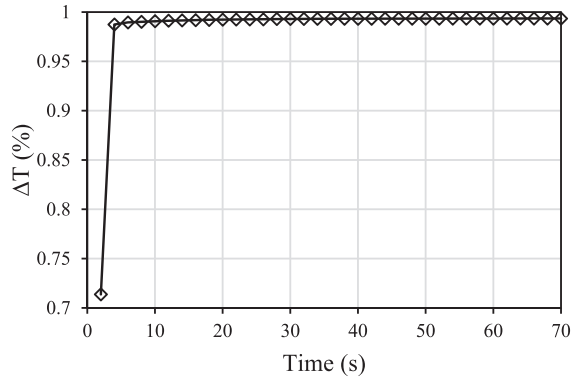
	J2	TI 1	TI 2	TO	BI	BO	Side	Lead
J1	1092	182	–	292	12	145	939	–
J2		–	198	249	13	537	–	271
TI 1			6150	–	–	–	5040	–
TI 2				–	–	3658	–	–
TO					–	–	147	1274
BI						–	–	–
BO							296	339
Side								202

Thermal capacities ($mJ{\cdot}K^{-1}$) of H-CTM.

J1	J2	TI 1	TI 2	TO	BI	BO	Side	Lead
2.2	1.9	0.6	0.6	3.1	3.0	1.9	2.8	1.8



GA convergence profile for DFN12 9 nodes CTM.



GA convergence profile for DFN12 9 nodes DCTM.

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