Mode Conversion in DC-DC Converters with Unbalanced Busbars

S. Negri, X. Wu, X. Liu, F. Grassi, G. Spadacini, S. A. Pignari
Dept. Electronics, Information and Bioengineering
Politecnico di Milano
Milan, Italy
{simone.negri}@polimi.it

***Abstract*—In this work, the undesired differential-to-common-mode conversion arising in low voltage DC-DC converter system due to busbar asymmetries with respect to the converter metallic case is investigated. To this end, a typical test setup for conducted emission (CE) verifications is modelled, which exploits two different DC-DC converter topologies. A circuit interpretation of the imbalance introduced by the busbar is provided in terms of differential and common mode equivalent circuits. The proposed simulation results allow putting in evidence the different impact of mode conversion on the DC-bus CM current for the two converter topologies under analysis.**

***Keywords*—Common and Differential Mode Noise; Conducted Emissions; DC-DC converters.**

I. Introduction

Power electronics systems have undergone a fast revolution in several energy-conversion frameworks, especially for large-scale renewable energy generation [1], [2]. However, the high-rate switching and non-ideal behavior of the involved circuit components are responsible for non-negligible electromagnetic interference (EMI), which may degrade the Electromagnetic Compatibility (EMC) performance of the electronic control systems [3]. Over the past years, several modeling tools and measurement techniques have been developed to predict and quantify the EMI noise generated by these devices (e.g., [4] and [5]), so to provide guidelines for EMC-oriented design of power converters and related EMI filters. One important aspect is related to the undesired noise generated by structural asymmetries of the converter with respect to the metallic case. Such structural imbalance with respect to ground usually leads to the generation of undesired common mode (CM) currents, which increase the overall conducted emissions (CE) exiting the converter. Several authors contributed to the evaluation of converter structural imbalance. In [6], [7] imbalance due to wide-bandgap semiconductor switches is analyzed through an equivalent-circuit-based model, allowing to quantify the resultant CM to differential-mode (DM) coupling. In [8], the impact of unbalanced EMI filter components, including CM capacitors and inductors, is investigated. In [9], a measurement-based technique for experimental characterization of unbalanced impedances is proposed.

In this work, the imbalance introduced due to busbar design and assembly with respect to the convert case is considered, and its impact on DM into CM conversion is investigated. Circuit simulations of a standard CE test setup involving two different DC-DC converter topologies are performed to reveal the (different) impact of the imbalanced due to the busbar on the generation of undesired CM currents on the DC bus.

II. Test Setup under Analysis

The EMC test setup analyzed in this paper is shown in Fig. 1. Two different configurations of the semiconductor module will be investigated: 1) a single-leg module, implementing a step-down converter; 2) a two-leg module, realizing a full-bridge DC-DC converter. For prediction in the CE frequency range [10], parasitic parameters of components have been included, as it will be discussed in the next section. Passive elements are identical for both configurations.

The converter is supplied through a standard line impedance stabilization network (LISN) [10], whose input is connected to a 200 V DC source. Similar switching conditions are assumed for both the aforesaid configurations, that is: switching frequency f_s = 10 kHz, constant duty cycle δ = 0.8, with unipolar modulation for the full-bridge. The 4 Ω resistor load is connected to the output filter through a balanced two-conductor (10 AWG) transmission line (TL), running 20 mm far from a metallic ground. The corresponding per-unit-length parameters were obtained considering a wire separation of 10 mm by using a 2D electrostatic solver.

III. Component Analysis and Modeling

A. Parasitic parameters

The nonideal equivalent circuit of the capacitors consists of the series combination of nominal capacitor, series resistor and inductor, as it is shown in Fig. 1. More specifically, electrolytic capacitors are assumed to be used as DC link capacitors and output filter capacitor, whose typical nominal capacitance (C_{el}, C_f), series resistance (R_{el}, R_{cf}) and series inductance (L_{el}, L_{cf}) are 6800 μF, 22 mΩ and 67.11 nH [11], respectively. For the decoupling capacitor, a metallized polypropylene film capacitor is assumed with nominal capacitance (C_{cd}) and typical series resistance (R_{cd}) equal to 1 μF and 2.7 mΩ, respectively. In order to estimate the value of its (parasitic) series inductance, the impedance of one sample is measured off-line by using a Keysight E4980A LCR meter. Once the resonant frequency f_0 has been obtained, the inductance value is calculated as:

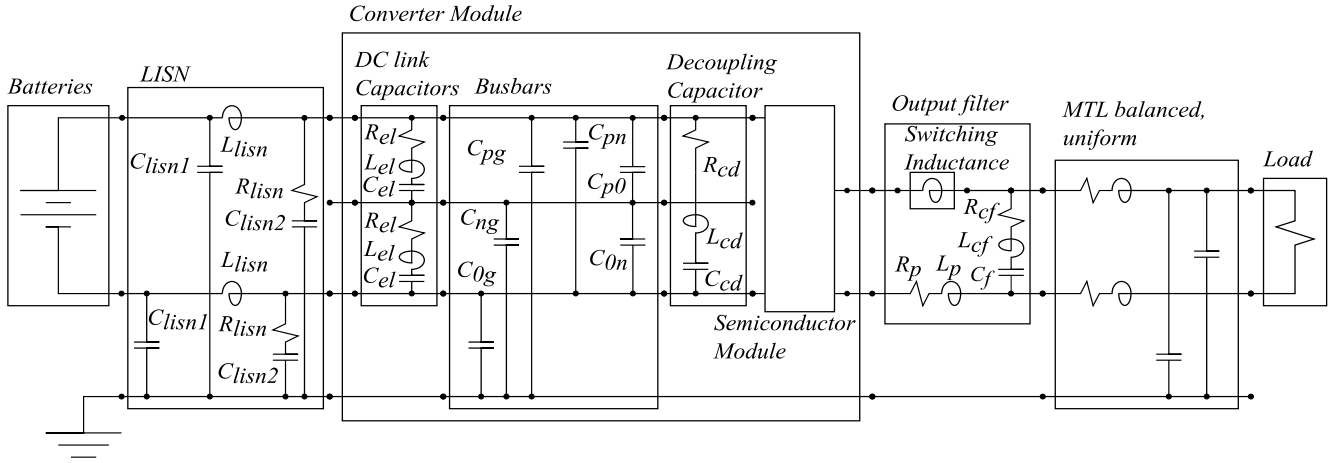


Fig. 1. Circuit modeling of the EMC test setup under investigation.

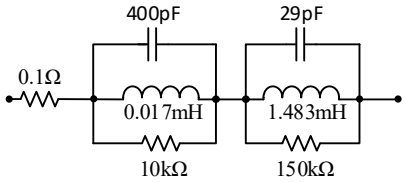


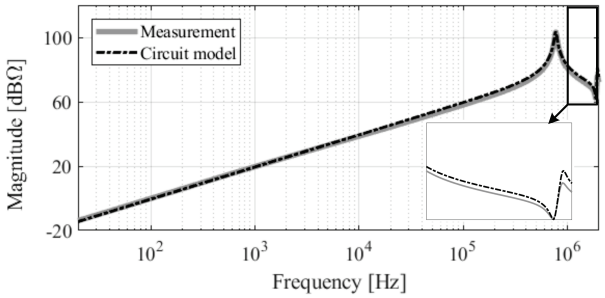
Fig. 2. Equivalent circuit model of the output inductor.

$$L_{cd} = \frac{1}{4\pi^2 f_0^2 C_{cd}} \tag{1}$$

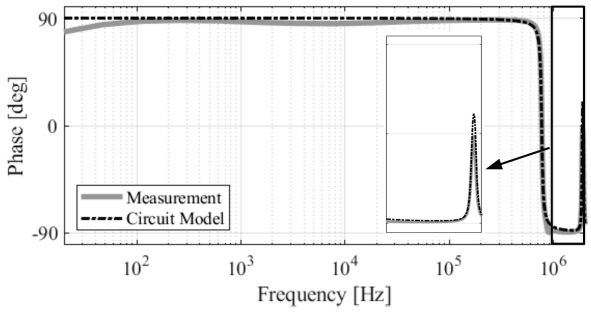
Similarly, for the output inductor, whose nominal inductance is 1.5 mH, the input impedance was measured off-line with the objective to properly model its non-ideal behavior. To this end, the equivalent network with topology and values of involved circuit components reported in Fig. 2 was adopted, which assures excellent fitting of the measured impedance as shown in Fig. 3.

B. Modeling the busbar

A typical industrial busbar design for low-voltage power converters is depicted in Fig. 4. From the 3D CAD model one can easily appreciate that the plus layer ("+"), the minus layer ("–") and the zero layer ("0") are in asymmetric positions with respect to the case, acting as reference ground. Indeed, the + and – layers are packaged as close as possible in order to minimize the busbar inductance. Such an asymmetry with respect to ground may worsen the CEs generated by the converter due to undesired mode conversion. To quantify the phenomenon, the 3D model in Fig. 4 (b) was firstly simulated by using the electrostatic module available in ANSYS Maxwell. Numerical simulation yielded the capacitance values listed in the first column of Table I. The effectiveness of the obtained values was then verified by measurement. To this end, the mutual capacitances of one busbar sample is measured by an ad hoc setup involving a 5-kV 50-Hz voltage source and a current probe. The obtained capacitance values (i.e., C_{0n} = 0.57 nF, C_{pn} = 0.7 nF) slightly exceed those obtained by simulation. The reason for this difference is probably to be ascribed to the fact that in the simulation model the air gap between the metal and dielectric layers is considered to be uniform, while in the measurement setup this is partially squeezed by plastic screws [see Fig. 4 (a)].



(a)



(b)

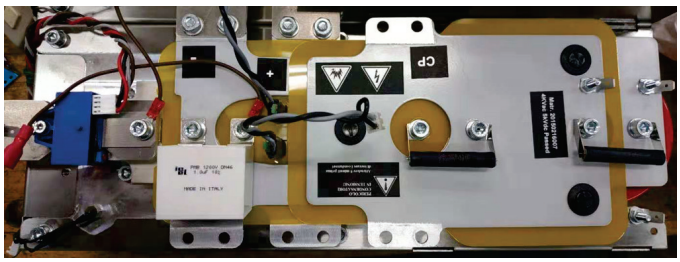
Fig. 3. (a) Magnitude and (b) phase of the impedance of the output inductor: Measurement vs prediction obtained by the model in Fig. 2.

To investigate the mode conversion introduced by the busbar asymmetric layout, differential mode (DM) and common mode (CM) quantities are introduced by the transformation matrices in [10]. Accordingly, the relationship between modal currents at the two ports of the busbar (see Fig. 1) are expressed as:

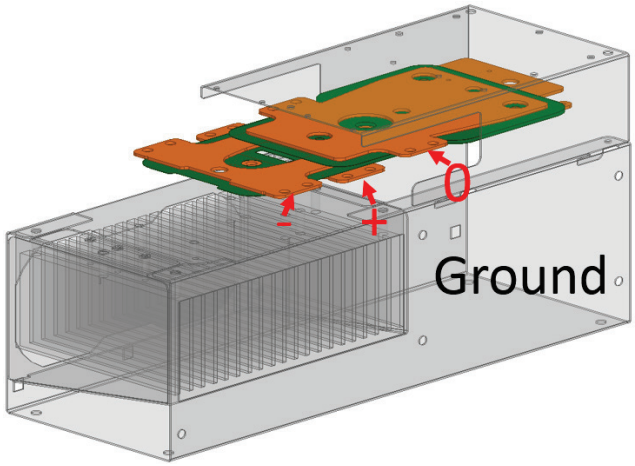
$$\begin{bmatrix} I_{DM}^{port1} \\ I_{CM}^{port1} \end{bmatrix} = \begin{bmatrix} I_{DM}^{port2} \\ I_{CM}^{port2} \end{bmatrix} - j\omega \begin{bmatrix} C_{DM} & \Delta C \\ \Delta C & C_{CM} \end{bmatrix} \begin{bmatrix} V_{DM} \\ V_{CM} \end{bmatrix} \tag{2}$$

where:

$$C_{DM} = \frac{C_{ng} + C_{pg}}{2} + 2C_{pn} + \frac{C_{0g}C_{0n}}{2(C_{0g} + C_{0n})} + \frac{C_{0g}C_{p0}}{2(C_{0g} + C_{p0})} + \frac{2C_{0n}C_{p0}}{C_{0n} + C_{p0}} \tag{3}$$



(a)



(b)

Fig. 4. (a) Picture and (b) 3D CAD model (with case) of the busbar under analysis.

$$C_{CM} = \frac{C_{ng} + C_{pg}}{2} + \frac{C_{0g}C_{0n}}{2(C_{0g} + C_{0n})} + \frac{C_{0g}C_{p0}}{2(C_{0g} + C_{p0})} \tag{4}$$

$$\Delta C = \frac{C_{pg} - C_{ng}}{2} - \frac{C_{0g}C_{0n}}{2(C_{0g} + C_{0n})} + \frac{C_{0g}C_{p0}}{2(C_{0g} + C_{p0})} \tag{5}$$

Thus, the DM and CM equivalent circuits of the busbar are those in Fig. 5, where undesired DM-to-CM conversion is included by the induced current source $\Delta I = -j\omega\Delta C V_{DM}$ [12].

TABLE I
BUSBAR CAPACITANCES

Capacitance	
C_{0n}, "0" to "-"	0.39 nF
C_{pn}, "+" to "-"	0.50 nF
C_{p0}, "+" to "0"	5.1 pF
C_{pg}, "+" to "ground"	9.25 pF
C_{ng}, "-" to "ground"	7.11 pF
C_{0g}, "0" to "ground"	9.22 pF

(a) (b)

Fig. 5. (a) DM and (b) CM equivalent circuit of the busbar under analysis.

IV. SIMULATION RESULTS

To evaluate the effect of busbar imbalance on the CM and DM currents injected in the DC bus, circuit simulations performed considering the actual busbar geometry in Fig. 4 are compared with those obtained by assuming the busbar as perfectly symmetric with respect to ground. In this case, each mutual capacitance between two busbar layers and each capacitance to ground are made equal to $(C_{pn} + C_{p0} + C_{0n})/3$ and $(C_{pg} + C_{0g} + C_{ng})/3$, respectively.

In the first set of simulations, a 2 m-long TL is assumed between the load and the output filter. The predicted CM and DM DC-bus currents injected by the step-down converter are plotted in Fig. 6 and Fig. 7, respectively. Unlike DM current (which is substantially unaffected), the amplitude of some switching harmonics (mainly around 80 kHz) in the CM current spectrum in Fig. 6 exhibits differences on the order of some decibels (with a maximum increase of 10 dB at 80 kHz). Since a step-down converter generates CM and DM harmonics at the same specific frequencies (i.e., integer multiples of its switching frequency), DM-to-CM conversion due to busbar imbalance is here appreciated in terms of increase in the amplitude of the CM harmonics.

This effect is even more visible if the full-bridge converter is considered. As a matter of fact, since in ideal conditions DM and CM current spectra exiting a full-bridge converter should involve exclusively even and odd switching harmonics, respectively, undesired mode conversion owing to busbar imbalance is responsible for the new even harmonics in CM-current spectrum in Fig. 8. Conversely, the DM current spectrum (see Fig. 9) is negligibly influenced.

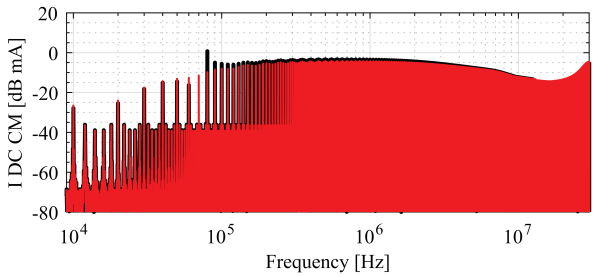


Fig. 6. Step-down converter, 2 m TL. CM current on the DC bus: Balanced (red) vs unbalanced (black) busbars.

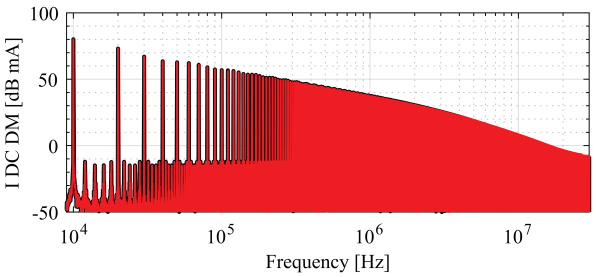


Fig. 7. Step-down converter, 2 m TL. DM current on the DC bus: Balanced (red) vs unbalanced (black) busbars.

To evaluate the impact of the TL length on mode conversion, simulations were repeated considering a 20-m long

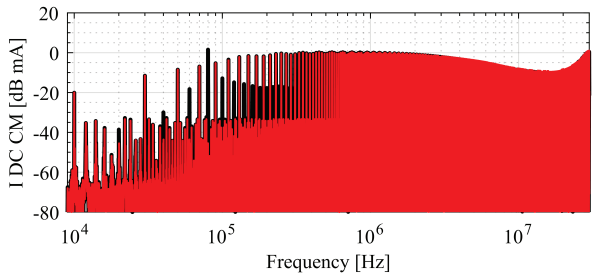


Fig. 8. Full-bridge converter, 2 m TL. CM current on the DC bus: Balanced (red) vs unbalanced (black) busbars.

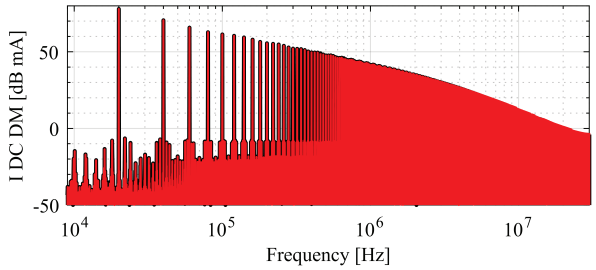


Fig. 9. Full-bridge converter, 2 m TL. DM current on the DC bus: Balanced (red) vs unbalanced (black) busbars.

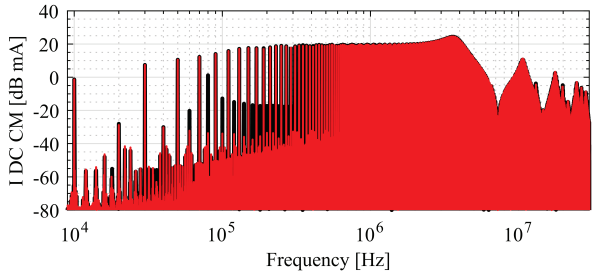


Fig. 10. Full-bridge converter, 20 m TL. CM current on the DC bus: Balanced (red) and unbalanced (black) busbars

TL. As an explicative example of the obtained results, Fig. 10 shows the comparison between the predicted CM DC-bus current injected by the full-bridge converter with balanced (red) and unbalanced (black) busbars. One can clearly notice that longer TLs generally result in higher CM currents, due to the reduced impedance to ground. Hence, as long as the TL is ideally balanced with respect to ground, the effect of busbar imbalance is less evident in the presence of longer TLs, since the CM generated by the converter (and magnified by the line presence) significantly exceeds the CM due to mode conversion.

V. Conclusion

In this paper, the effect of busbar imbalance on CM/DM noise generated by power electronics converters has been investigated. To this end, a typical CE test setup involving two different DC-DC converter topologies has been accurately modeled and simulated. Simulation results showed significant CM noise generated through DM-to-CM conversion due to busbar imbalance. This effect is particularly evident in the case of a full-bridge converter, due to the different harmonic content of CM and DM noise spectra, as well as in the case of shorter TLs.

Acknowledgment

The Authors gratefully thank Mr. Giovanni Ubezio and Energy Components & Consulting S.r.l. for the data kindly shared.

References

[1] F. Blaabjerg, Z. Chen and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184-1194, Sept. 2004.

[2] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. Portillo Guisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso., "Power-electronic systems for the grid integration of renewable energy sources: a survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002-1016, June 2006.

[3] Q. Liu, S. Wang, A. C. Baisden, F. Wang, and D. Boroyevich, "EMI suppression in voltage source converters by utilizing dc-link decoupling capacitors," *IEEE Trans. Power. Electron.*, vol. 22, no. 4, pp. 1417–1428, Jul. 2007.

[4] Q. Liu, F. Wang and D. Boroyevich, "Modular-Terminal-Behavioral (MTB) model for characterizing switching module conducted EMI generation in converter systems," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1804-1814, Nov. 2006.

[5] R. Trinchero, I. S. Stievano and F. G. Canavero, "EMI modeling of switching circuits via augmented equivalents and measured data," in *Proc. 2015 IEEE Int. Symp. Electromagn. Compat.*, 2015, pp. 130-133.

[6] A. D. Brovont and A. N. Lemmon, "Common-mode/differential-mode interactions in asymmetric converter structures," in *Proc. 2017 IEEE Elect. Ship Technol. Symp.*, 2017, pp. 84-90.

[7] A. D. Brovont, "Generalized differential-common-mode decomposition for modeling conducted emissions in asymmetric power electronic systems," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6461-6466, Aug. 2018.

[8] S. Wang and F. C. Lee, "Investigation of the transformation between differential-mode and common-mode noises in an EMI filter due to unbalance," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 3, pp. 578-587, Aug. 2010.

[9] H. Zhang and S. Wang, "EMI noise source modeling based on network theory for power converters with mixed-mode characterization," in *Proc. IEEE Appl. Power Electron. Conf. (APEC '18)*,2018, pp. 984-991.

[10] C. R. Paul, *Introduction to Electromagnetic Compatibility*, Wiley Interscience, NY: New York, 1992.

[11] Itelcond AYX-HR series electrolytic capacitors. http://www.itelcond.it/wp-content/uploads/2017/11/03-Serie-AYX-2018.pdf.

[12] F. Grassi, Y. Yang, X. Wu, G. Spadacini, S. A. Pignari, "On mode conversion in geometrically unbalanced differential lines and its analogy with crosstalk," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 2, pp. 283-291, Apr. 2015.