High energy pulsed laser deposition of ohmic tungsten contacts on silicon at room temperature

D. Dellasega[1], M. Bollani[2,*], L. Anzi[3], A. Pezzoli[1], D. Chrastina[3], A. Gulinatti[4], G. Irde[5], R. Sordan[3], M. Passoni[1], and S.M. Pietralunga[6]

1 Dipartimento di Energia, Politecnico di Milano, via Ponzio 34/3, 20133 Milan, Italy

2 L-NESS, IFN-CNR, Via Anzani 42, 22100 Como, Italy.

3 L-NESS, Dipartimento di Fisica, Politecnico di Milano, Polo di Como, Via Anzani 42, 22100 Como, Italy

4 Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, via Ponzio 34/5, 20133 Milan, Italy

5 Dipartimento di Fisica, Politecnico di Milano, Piazza Leonardo da Vinci 32, 20133 Milano, Italy

6 IFN-CNR, Piazza Leonardo da Vinci 32, 20133 Milano, Italy

* corresponding author: monica.bollani@ifn.cnr.it

Abstract

Tungsten-on-n^+ silicon ohmic contacts were obtained by depositing 100 nm-thick W coatings on silicon substrates using pulsed laser deposition at room temperature, without native oxide removal. The high energy of the impinging species (about 10-100 eV per atom) led to sputtering phenomena and to the implantation of W atoms through the Si oxide. W coatings were characterized, as-deposited and after performing rapid thermal annealing steps. The morphology and crystallinity were characterized by scanning electron microscopy, X-ray diffraction and reflectometry. The interdiffusion of W and Si was shown by scanning Auger microscopy. The ohmic character of the contacts and contact resistance were investigated by the transfer length method. Fast annealing at moderate temperatures (450 °C) remarkably improved contact performance without significant variation of the features of either W film or Si substrates. The ohmic character of the contact was preserved even after annealing at high temperature (1000 °C) at which a complete interdiffusion of Si into the W film takes place.

Introduction

Tungsten is used in microelectronics since decades, to provide metallic contact on Si and wide band-gap semiconductors such as silicon carbide [1–4]. It features complementary metal oxide semiconductor compatibility, a high melting temperature, useful to sustain the chemical vapor deposition (CVD) processes typical of very large-scale integration (VLSI) technology and to guarantee the thermal stability of the contact, high mechanical and chemical resistance as well as high adhesion and wettability on silicon. Specifically, the latter properties make it a material of choice for the metallization of high aspect ratio patterns and through-silicon vias (TSV) [5,6]. It also features the best matching of thermal expansion coefficient with Si. Its electrical resistance is comparable with Al, Cu and noble metals. In addition, thanks to its low electron mean free path (19 nm), in the case of very thin films, W exhibits lower resistivity compared with other metals, like e.g. Cu [7].

The metal-semiconductor abrupt junction at Tungsten on (001) Silicon surface is characterized by Schottky voltage barrier heights around 0.7 eV and 0.5 eV, respectively in case on *n*-type and *p*-type doped Si [8,9]. Due to these high values, in the case of pure W-Si system an ohmic contact can be established only with the contribution of quantum tunneling effects. Tunneling probability and, as a consequence, the value of contact resistivity for the ohmic contacts depend in turn on the width of the voltage barrier, which is a function of the dopant concentration in Si [10]. Only at very high doping concentrations, higher than 10^{20} cm^{-3}, the establishment of a reliable tunnel current occurs [11].

To overcome this problem at lower doping levels several recipes have been developed to obtain W-on-Si ohmic contacts, which mostly rely on depositing W either in alloys or in metallic multilayers, such as WN/W/PtSi/Si or W/TiN/TiSi/Si structures. Refractory metal silicides are considered as alternative materials for low-resistance ohmic contacts and interconnects on Silicon in VLSI systems [12]. Tungsten silicide, specifically WSi_2, is a metallic compound, forming a barrier with Silicon substrate, which strongly depends on the conditions of W deposition and subsequent annealing. Reported values for the height of the WSi_2/n-Si barrier range from 0.68 eV to 0.86 eV [13]. Tungsten silicides may be either directly deposited, or formed by a post-deposition annealing step at high temperature (above 650°C, see [14,15]). W silicides have beneficial effects by promoting the adhesion of the W metallic layer on Si. Moreover they act as a diffusion barrier for the silicon and ensure a higher conductivity compared with polysilicon [4,16–18] and favor the ohmic contact.

It would be of technological interest to diminish the number of process steps necessary to obtain W on Si ohmic contacts by depositing W directly on Si. To overcome the problem of Si doping, a W-Si intermixed zone can be created at the interface using high energy species. Ion-assisted metal deposition on Si results in graded composition interfaces, leading to non-rectifying low-resistance contacts, as has been demonstrated at a local scale by direct writing of tungsten contacts using focused ion beam (FIB) assisted techniques [19–21]. Therefore, differently from the W multilayered systems, the direct deposition of W on Si may lead to the formation of ohmic contacts without the need for thermal annealing steps. This, in turn, would be beneficial with respect to the total thermal budget of the production process. Moreover, high temperature processing steps may induce the migration of the dopant species, thus affecting the performances of the device.

One further major issue related to the fabrication of ohmic W-Si junctions is the presence of native oxide on Si surface. The presence of interfacial oxide significantly retards the formation of W-Si compounds, and leads to the absence of a good electrical contact [11,14,22]. During the deposition of W by chemical vapor deposition (CVD) the grow rate and even the crystallographic phase of the deposited W film are influenced by the thickness of native silicon oxide [23]. If a barrier to WSi_2 formation exists due to the native oxide, incomplete substrate covering by deposited W occurs and non-uniform layer is formed [14]. Due to the difference in coefficient of thermal expansion between W and Si oxide (respectively 4.5 and 0.55 μm /m K) stress, delamination or even detachment of W film may happen during the deposition procedure if native silicon oxide has not been removed [24]. Finally this issue becomes important whenever very high aspect ratio structures are considered, as in TSV connections, where, however, complete oxide removal is hardly achieved [25]. For all these reasons, a process step of native oxide removal usually needs to be performed before depositing the W coating, to assure reliability and uniformity in deposition and to improve contact performances.

W films are deposited by one out of several different techniques, depending on the application envisaged. Magnetron sputtering [1,3], CVD [26,27], and e-beam evaporation [28,29] are mostly used. In the present work, tungsten contacts have been deposited by Pulsed Laser Deposition (PLD) technique on (001) n^+ Si substrates. Specifically, in this work we show that, by directly depositing W on Si contacts using PLD, ohmic electrical character can be obtained, starting from room temperature conditions, without requiring extremely high doping levels for the Si substrate and without the need to remove the native oxide layer at Si surface.

PLD is an out-of-equilibrium physical vapor deposition technique which, although mainly exploited for the deposition of metallic oxides [30], has proven to be also very effective in depositing pure metallic films (e.g. Rh films [31]). By exploiting the non-equilibrium features of the PLD process, metallic tungsten film structures ranging from nanocrystalline columnar to amorphous-like and porous can be grown [32]. The proper thermal annealing of amorphous-like W may even induce the nucleation and growth of tungsten-oxide nanowires [33]. During the PLD process, when a laser fluence higher than 10 J/cm^2 is used, ions and atoms impinge on the sample surface with energies of about 10-100 eV [34,35], what may lead to sputtering of the surface and implantation and diffusion phenomena in the substrate [36,37]. Therefore, similarly to what occurs in the case of FIB-assisted W deposition, PLD could contribute to improve the contact features of W directly deposited on Si on a large, macroscopic, scale. The high energy regime of PLD would allow the deposition of adherent coatings and the thinning or removal of native oxide at surface. The advantage would be twofold: to reduce the disadvantages related to the presence of oxide and, at the same time, to avoid the need for a dedicated removal step in the production process. In addition, the implantation of W atoms in Si surface could influence the formation of WSi_2 layer after annealing, thus improving the performances and stability at high temperature. Thanks to the high energy of the impinging species, deposition by PLD might be suitable to grow metal contacts onto high aspect ratio channels and patterned surfaces. Actually, recent studies on black silicon solar cells, that rely on deep roughening of the top surface to enhance sunlight absorption [38,39], prove that Ti/Pd/Ag ohmic contacts deposited by PLD onto the rough surface outperform those deposited by other techniques (sputtering, thermal evaporation, direct printing) [39]. On the other side, PLD should be strictly taken as a prototypical technique, suffering of issues related to the limited deposition area and the possible presence of droplets. In the case deposition at high energies turns out to be a key asset to

reach desired features of the metallic contacts, large scale deposition processes can eventually be devised, by turning to more industrially scalable high energy techniques, such as High Power Impulse Magnetron Sputtering with a proper bias voltage [40].

We deposited W on Si contacts by PLD at room temperature and performed Rapid Thermal Annealing (RTA) steps at various temperatures, up to 1000° C. Systematic electrical and structural characterizations have been carried out after annealing from room temperature up to 1000°C observing the silicide formation and Si interdiffusion.

Experimental details

W coatings were deposited by PLD [32], by exploiting the second harmonic of a Nd:YAG laser at λ= 532 nm, repetition rate of 10 Hz, temporal pulse duration of 5-7 ns and energy per pulse of 740 mJ. The spot area of the impinging laser on the target was about 5 mm^2 and the measured fluence ~ 14.5 J/cm^2. The species ablated from the W target expanded in the deposition chamber, at a base pressure of 3×10^{-3} Pa. In this pressure regime the main important gas contaminant is oxygen. The expanding species, mainly single atoms under the conditions of ablation above described, were collected on the substrate positioned 70 mm away from the target. Thanks to the use of a sample holder which keeps the substrate in motion during the deposition, and to an off–axis deposition scheme [31], the deposition of a uniform W film was achieved. In the present deposition conditions, the growth rate turns out to be 14.3 nm/min. Film specimens 50 nm thick were deposited on plain Si substrate, for structural characterization. W film 100 nm thick were deposited on n^+ type Si for the electrical characterization of the contacts. After deposition, W films and contacts were subjected to RTA in N_2 atmosphere at 200°C, 450°C, 850°C and 1000°C, with a dwell time of 5 min.
Film morphology has been characterized by a *Zeiss Supra 40* field emission scanning electron microscope (SEM) with an accelerating voltage of 3 - 5 kV. The film crystalline structure has been analyzed by X-ray diffraction (XRD) and reflectivity (XRR) using a *PANalytical X'Pert PRO MRD* X-ray diffractometer (monochromatic Cu Kα1 radiation, λ = 0.1540562 nm). Local compositional analysis in depth profiling of the Si-W interface region was performed by UHV Scanning Auger Micro-spectroscopy (SAM) *(PHI 660).* Depth profiling was performed by sputtering the W coating with Argon ion gun (V = 4 kV, I = 2 μA). The content in Si and W at exposed surface was rated by measuring the Silicon LMM Auger peak at 96 eV and Tungsten NNN peak at 180 eV. Oxygen content was also estimated, by counting the O KLL line at 510 eV, while checking for the content of Carbon contaminant by its KLL line at 250 eV. Measurements were taken at V=3 kV of accelerating voltage, I = 30 nA of electron beam current and with an energy resolution of $\Delta E/E$ = 1%. Under present experimental conditions, depth sensitivity of Auger analysis is between 1 and 2 nm, as limited by electron effective attenuation length, calculated using the NIST SRD 82 database software [41].
For the W-on-Si contacts electrical characterization n^+ type (As-doped, resistivity 1-4 mΩ·cm) Si (001) substrates were used. Native oxide, of estimated thickness around 0.7 – 1.5 nm [42], was not removed from the Si surface. A sequence of W rectangular electrodes was fabricated by optical lithographic and lift-off procedure, in a typical transfer length method (TLM) structure used to characterize n or p type Si or n-p type Si-Ge films as reported in [43] [44] the TLM is, indeed, an useful approach to describe the planar contacts between a metal and semiconductor material. The sequence of definition of the W-on-Si electrodes is illustrated in Figure 1. The thick resist film, pre-patterned by optical lithography, was coated with W PLD films, 100 nm thick. Then a lift-off step

in acetone was performed to remove the resist and to define the electrodes. In the resulting TLM geometry, each electrode measured 48 μm × 200 μm and the inter-electrode distance increased from 15 to 65 μm (see Figure1). I-V characteristics of the W on Si system were measured and specific contact resistivity (ρ_C) was extracted using the TLM approach on the patterned W contacts [45].

Results

Film morphology after the different annealing treatments was assessed by SEM. As shown in Figure 2a (not-annealed film), the deposited W film is very smooth and compact, thanks to the high energy of the impinging species and the nanocrystalline domains are clearly visible. The annealing at 450°C does not significantly affect the morphology of the film. Also, the dimensions of the crystallite domains are unchanged. The thermal treatment at 850°C results in the development of a completely different morphology. The surface appears much rougher and irregular made of nanoaggregates. The annealing at 1000°C induces the same kind of morphology although the nanoaggregates are more defined and nano-crystalline facets start to appear.

Figure 3 compares measured XRR spectrum of the deposited W film, 50 nm thick, with a dynamical simulation [46], vertically offset for clarity. The simulation (reduced chi-squared: 0.0035) specifies a film thickness of 52.5 nm, with a surface roughness of ~ 0.9 nm. The agreement in critical angle between the measurement and the simulation indicates that the density of the deposited layer is equal to that of W, i.e. that the deposited film is compact and not porous.

Figure 4a, shows a wide 2θ scan XRD analysis at grazing incidence for the W film (50 nm thick) following annealing at different temperatures. Only the reflections related to the crystalline α-W phase (and some asymmetric Si reflections from the substrate) are visible. The W film annealed at 450°C behaves similarly to the as-grown material without annealing (not shown here). On annealing at 850°C the diffraction pattern changes completely to that of tetragonal WSi_2 with no carbides or oxides of tungsten visible, but then there is no further change on annealing up to 1000°C. In Figure 4b a detailed 2θ-ω scan around the α-W (110) peak is shown. The results confirm the close resemblance of the diffraction patters of the as-grown W film and of the specimen annealed at 450°C, suggesting that the material is already heated by the PLD process and that the annealing at 450°C would not affect the crystallinity of W, because of the short dwell time and low temperature. On the other hand, both in the case of the as-grown film and material annealed at 450°C, a weak broad peak at 47° is evident, which may correspond to the presence of a small amount of WO_3. XRD cannot, however, confirm the presence or absence of a thin layer of amorphous SiO_2 at the W/Si interface. The complete transformation of W 50 nm thick into WSi_2 after a so short annealing (dwell time 5 minutes) at 850°C is an indirect proof of a deep change in the properties of the W-Si interface. In fact as reported in [14] the presence of the native oxide layer should have prevented the diffusion of Si in the W film.

To better address this point, elemental analysis across the W-Si interface for W films 100 nm thick was performed by depth profiling (by means of sputtering) SAM. Figure 5 shows the compositional profile taken in a line across the sputtered region, for the not-annealed sample. W, Si and O relative concentrations across the W-Si interface, from 20 nm in the bulk of the W film to 70 nm in the bulk of Si substrates, are shown. The depth of the sputtered zone was calibrated by profilometry. It is worth to note that the depth sensitivity of SAM is about 1 nm and thus the O concentrations are

related to the surface contamination. The impurities may be related to the measurement setup or incorporated in the W film during the deposition. A significant implantation of W into the Si substrate has taken place during PLD generating an intermixing zone of about 20-30 nm, due to the high energy of the impinging W species. It is interesting to note that there is no variation in the oxygen signal at the W/Si interface. The state of oxidation of Si can be verified by checking the spectral shape of the Si Auger line at 96 eV. The Si spectrum taken all over the interface region of the sample at RT is reported in the inset of Fig.5 and corresponds to unoxidized crystalline Si, showing that the native silicon oxide layer has been removed during the PLD process.

The evolution in depth of the W/n^+ Si compositional ratio is reported in Figure 6, at room temperature and after 850 °C thermal annealing. In the as-deposited sample W concentration is 100% in the W film and rapidly decreases going into the Si substrate generating an intermixing zone of 20 – 30 nm. The presence of implanted W in Si is likely to occur during the PLD process at laser fluences higher than 10 J/cm^2 [36]. On the contrary, in the case of W films deposited by sputtering on Si-based substrates, ohmic contact is possible only after high temperature annealing that leads to the formation of W inter-metallics [4]. RTA at 850°C does not affect the composition of the intermixing zone under the Si surface. In fact, the differences in relative composition are negligible. But the RTA at 850°C increases Si concentration (W signal decreases) in the W film, which is an indication of Si interdiffusion up to the surface. The result of RTA at temperatures higher than 850°C results in a diffusion of Si from the substrate up to the surface of the film corresponding to the formation of WSi_2. It is interesting to note that due to the increased thickness of the W film, 100 nm instead of 50 nm, the short annealing time (5 min.) did not allow the diffusion of a sufficient amount of Si to induce the complete formation of WSi_2 as shown in the case of the W films 50 nm thick annealed in the same conditions.

I-V characteristics of the W-on-Si system were measured and specific contact resistivity (ρ_C) was extracted using the TLM approach on the patterned W contacts [45]. Figure 7a) reports the I-V characteristic measured between two electrodes (inter-distance of 25 μm) of the TLM geometry, before performing any additional thermal treatment. The I-V curve is linear in the whole measurement range. Moreover, the linear trend of I-V curve indicates that the native oxide has been modified or is no longer present.
Transport through a native oxide layer of three different thicknesses was simulated with a direct tunneling model, Sentaurus Device from Synopsys [47], in Figure 7 b). The simulated I-V characteristics are all strongly nonlinear. The linearity of the experimental I-V characteristic, in this case, can be ascribed to the implantation of W atoms in the silicon substrate as shown in the Auger analysis. The W-Si intermixing zone allows the establishment of an ohmic contact between the metal and semiconductor.
In Figure 8 a) the I-V characteristics of the TLM resistor after thermal annealing are reported. The total resistance (R_T) of the contact can be extracted from the slope of I-V curve. The R_T can be modeled as the sum of three components:

$$R_T = 2\,R_m + R_S + 2\,R_C$$

where $2\,R_m$ represents the internal resistance of the two metallic conductors, the R_S is the semiconductor resistance and the $2\,R_C$ represents the contact resistance between the metal and semiconductor for two metallic contacts, as reported in [43]. Typically, $R_m$is negligible when

compared to the other terms, while the term R_S is very small due to the high conductivity of n^+ Si. It is evident from Figure 8 a) that there is a significant reduction in R_T, because of thermal annealing. From what stated before, we can conclude that this is a consequence of a lowering in resistivity of the contacts as the annealing time is too small to affect the dopant distribution in Si. Due to strong dependence of the R_C on the contact area (A), it is appropriate to introduce a specific contact resistance ρ_C (Ωcm^2):

$$R_C = \frac{\rho_C}{A}$$

The different values of the R_C obtained by TLM measurements can be extracted by the characteristics in Figure 8a and the specific contact resistances ρ_C as a function of the annealing temperature are plotted in Figure 8b.

Experimental I-V curves shown in Fig. 8a are linear and symmetrical, indicating ohmic electrical conduction and, specifically, the ohmic behavior of the W/Si contacts.

The values for ρ_C, measured in the sample before and after annealing at 200°C ($\rho_C \sim 10^{-2}\ \Omega\cdot cm^2$) are very high compared to W/Si ohmic contacts deposited without native oxide (10^{-5} – $10^{-6}\ \Omega\cdot cm^2$)[11]. The introduction of a 5 min annealing step at moderate temperatures (up to 450°C) results in a lowering of ρ_C by one order of magnitude ($10^{-3}\ \Omega\cdot cm^2$), without inducing modifications in the crystallinity or stoichiometry of the deposited W layer, as shown by the XRD and Auger characterizations. A similar change in resistivity in the same temperature range has been found in W layers produced by FIB assisted CVD [19]. Ion bombardment produces an intermixing region between W and Si that is very sensitive to temperature variations [20]. The same temperature sensitivity has been found in the deposition of Fe-Si metallic contacts by PLD on silicon [48]. In that case the establishment of the ohmic contact is found to be dependent on the Fe-Si deposition temperature, promoting the diffusion of Fe atoms in the first substrate layers. After 5 minutes of annealing at 850°C or 1000°C the complete interdiffusion of Si in the W layer takes place, as shown in Figure 6. Correspondingly, the values for ρ_C decrease by almost one additional order of magnitude if compared with W annealed at 450°C, reaching $\sim 4\cdot10^{-4}\ \Omega\cdot cm^2$. Table 1 reports a comparison of the experimental ρ_C values obtained in this work with those featured by direct ohmic W/Si contacts fabricated using several deposition techniques, with and without thermal annealing process. Temperature and duration of the annealing is also reported. Results are given as order-of-magnitude evaluations. Tungsten coatings deposited using PLD, both at RT and annealed at low temperature, perform equivalently to W/Si contacts fabricated by FIB (respectively $10^{-2}\ \Omega\cdot cm^2$ and $10^{-4}\ \Omega\cdot cm^2$) and measured on structured contacts in a Cross-bridge Kelvin resistor scheme. Resistivity of RF-sputtering on plane substrates is lower compared with PLD, being around ($10^{-6}\ \Omega\cdot cm^2$). CVD exhibits even lower contact resistances (10^{-7} - $10^{-8}\ \Omega\cdot cm^2$) thanks to the selective removal of native oxide directly performed at the first stages of the deposition. It is worth to note that W contacts deposited by CVD are obtained using a Si substrate with a doping concentration of 10^{20} (cm^{-3}).

Ohmic I-V characteristics, as experimentally verified in the present case (see Figs. 7a and 8a), can be justified by a lowering of the voltage barrier that is established between metal and semiconductor. The electrical conduction across a metal--n-type semiconductor junction can be described with the aid of the sketch in Figure 9. At equilibrium conditions, in the Schottky limit

case (low density of interfacial defects) [49] a voltage barrier ϕ_{Bn} develops at the interface as $q\phi_{Bn} = (q\phi_m - \chi_s)$, where $q\phi_m$ is the metal work function and χ_s is the electron affinity for semiconductor. Vacuum energy level E_{vac} is also indicated, as well as Fermi energy levels, respectively named E_{Fm} for the metal and E_{Fn} for the semiconductor. On the semiconductor side, $q\phi_F$ is the distance in energy between the conduction band minimum and the Fermi level, according to semiconductor doping level. In dependence on the value of ϕ_{Bn} and on doping level, three different charge transport regimes can be identified to contribute to ohmic conduction [10][49]. In case of light semiconductor doping, the ohmic behavior of the contact is provided by thermionic emission of hot ballistic electrons over the barrier (TE regime). If very high doping levels are considered, close to degeneracy, the leading mechanisms is the emission of electrons by quantum tunneling across the barrier, driven by applied electric-field (Field-Emission FE regime). At intermediate doping levels charge conduction can be modelled by a combination of the two regimes (Thermionic-Field-Emission TFE model). The Padovani-Stratton parameter is an equivalent energy defined as:

$E_{00} = \frac{e\hbar}{2}\sqrt{\frac{N_d}{m^*\epsilon}}$, where Nd is the donor concentration, $\hbar$ the reduced Plank constant, m* (≅0.5 m) the effective mass of electron and ϵ the dielectric permittivity of Si. The ratio E_{00}/kT measures the relative importance of the electron tunneling mechanism over the thermionic emission [Yu] and defines the regime of conduction between FE ($E_{00}/kT \gg 1$) and TE ($E_{00}/kT \ll 1$). Values $E_{00}/kT \sim 1$ indicate the intermediate TFE condition. The resistivity range of the n+ Si substrates used (1-4 mΩ cm) corresponds to donor doping densities $1.6 \div 8 \cdot 10^{19} cm^{-3}$ [10] and to $\frac{E_{00}}{kT} = 0.95 \div 2.12$ at T=298 K, so that electrical conduction across the barrier is TFE dominated [49].

Although in the present case an intermixed W-Si region is present, we use the model presented above to calculate an equivalent barrier height at the junction. The barrier height ϕ_{Bn} can be calculated [50] by comparing ρ_c values and by assuming Yu's TFE theory [49]. The obtained results are displayed in Table 2 in correspondence to the different annealing conditions of the W-Si system at low temperature, i.e. no silicide formation. If we compare the values obtained for ϕ_{Bn} with the Schottky limit case, we find a good agreement. A value $q\phi_{Bn} = (\phi_m - \chi_s) = 0.55\ eV$ can be estimated considering a work function value $q\phi_m = 4.6\ eV$ for polycrystalline W film [51] and $\chi_s = 4.05\ eV$ for electron affinity of Si [52]. However, in the present case of film growth by PLD the high energy of deposited W species will induce the formation of defects in the interfacial region. The presence of defects at the surface of a semiconductor results in the pinning of the Fermi energy level and in the departure from the Schottky limit model [10]. In this frame, the experimental values of about 0.7 eV for voltage barriers at abrupt W/n-Si interfaces are justified, leading to non-ohmic contacts [8,9]. In the PLD case, W implantation and the formation of an interdiffusion layer also introduce bulk deep intragap defect levels, of both donor and acceptor type [53,54]. At extremely high W concentrations, as reached in the intermixing zone, defect levels are likely to merge and to form intragap bands, which may also result in bandgap narrowing (see for instance [10]). Also, the formation of low bandgap WSi_x clusters in the intermixing zone is possible [55]. Accordingly, the W-Si system may display a barrier reduction also due to the fact that the bandgap of crystalline W silicide is about 0.3-0.4 eV [56]. A similar result is also suggested by the increase in the amplitude of the reverse current, occurring in the case of thermal interdiffusion of W into Si operated in Silicon diodes [53]. In Table 2, the conductivity improvement at 450 °C

annealing could be ascribed to an ordering of the alloyed W-Si intermixing region and corresponds to an equivalent barrier height of 0.35 eV, if TFE conduction model and all related parameters are kept as valid.

It is worth stating that the mechanisms ruling the barrier height at metal-semiconductor interfaces refer to the physical chemistry of surface at the atomic level and can still be considered as open field of investigation [57]. Mostly, in the present case a proper modelling of the W-Si intermixing zone would evidently be needed for a detailed explanation of electron transport. In fact, the interfacial region is deeply altered by interdiffusion and alloying, so that phenomena such as bandgap reduction, dopant activation and eventually WSi_2 crystallization at higher temperatures [58] can contribute both to a reduction in voltage barrier and to variations in the mechanism of ohmic conduction itself.

Conclusions

In this work we characterized the structural, morphological and electrical properties of W contacts, deposited at room temperature on n^+ Si wafers using PLD and which turn out as compact, polycrystalline α-W films. Due to the high energy of the impinging species, interdiffusion of W in the Si substrate occurs. The metal-semiconductor contact across the W/n^+ Si interface exhibits an ohmic behavior prior to any thermal annealing step and without the removal of native oxide from the substrate. Fast low temperature annealing lowers contact resistivity without modifying the W film crystallinity, probably due to modifications of the W-Si intermixing region. Rapid thermal annealing at high temperature results in the complete interdiffusion of Si in the W film and WSi_2 formation, which further reduces the contact resistance. We consider that this deposition technique, due to the high energy of the impinging species, is likely to allow the coverage and the formation of W ohmic contacts on C-MOS compatible complex structures.

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List of Figures

Figure 1: Schematic sequence of the fabrication steps of W structures on Si substrate (not in scale). A thick photo resist was spin coated on a clean Si (001) surface. Then by optical lithography, rectangular patterns were defined in the photo resist, at different distances for TLM measurements. Without removing the native oxide, 100 nm of W film was deposited by PLD. Finally, a lift off process in acetone solution to remove the resist mask was used.

Figure 2: Planar view SEM images of W film 100 nm thick deposited by PLD. As deposited a), after annealing at: 450°C b), 850°C c) and 1000°C d). The film roughness increases as the temperature increases due to the formation of silicides.

Figure 3: XRR analysis of a 50 nm W film deposited on Si, as compared to a dynamical simulation of a 52.5 nm film with 0.9 nm surface roughness (offset vertically for clarity).

Figure 4: XRD analysis of W on Si for various annealing temperatures. (a) a grazing incidence (ω=5°) scan with an "open" detector (acceptance of approximately 2°) gives an overview of the film properties. Following annealing at 450°C the film is very similar to the as-deposited material (not shown). Following annealing at 850°C, the film transforms completely to WSi_2 with no carbides or oxides of tungsten visible. The 2θ-ω scan (b) around the α-W (110) peak was performed in "triple-axis" mode with an analyzer crystal in front of the detector, and with this increased resolution and signal-to-noise ratio it is possible to see a weak broad peak (at 47°) possibly corresponding to the presence of a small amount of WO_3.

Figure 5: SAM depth profiling, across the W-Si interface, of 100 nm thick W on Si films deposited by PLD at RT and not annealed. Relative elemental composition is reported, and the oxygen content is also traced. An intermixing W-Si zone ranging 20-30nm is evident. The detection of contaminant oxygen does not correspond to any oxidation of the Si, as explained in the text. The minimum

detectable value in concentration corresponds to 2-5% sensitivity in detecting elemental composition, under present experimental conditions. The detected Auger spectrum of the Si peak at 96 eV is shown in the inset.

Figure 6: Relative W/Si composition, across the W-Si interface, for 100 nm thick W on Si films, deposited by PLD. Comparison between the composition in as-deposited film and after 5 min RTA step at 850° C is shown. The existence of an intermixed W-Si zone below the Si surface is common to both configurations, the extension and composition of which is not affected by RTA step. The RTA-processed sample shows a reduced W/Si ratio in the thickness of the W coating, indicating the thermally activated inter-diffusion of Si towards the surface.

Figure 7: a) Experimental I-V characteristic measured on a resistor of the TLM structure (electrodes separation = 25 μm). The linear fit made on this curve report a R-square value of 0.99983. b) Simulated IV characteristic of a one-dimensional $W/SiO_2/Si$ contact (area 200 μm x 48 μm) for different values of the native oxide thickness (t_{ox}).

Figure 8: a) The I-V characteristics of the TLM resistor at the different annealing temperature ranging from 200°C to 1000°C. b) Specific contact resistivity as a function of the annealing temperature.

Figure 9: Energy band diagram of a metal n-type semiconductor junction at equilibrium, in the Schottky limit and related ohmic conduction models. (a): The voltage barrier ϕ_{Bn} is formed as a function of the difference between the metal work function and the electron affinity for the semiconductor; (b): Very high doping : $\frac{E_{00}}{kT} \gg 1$, Field Emission (FE) conduction regime through quantum tunneling; (c): Light doping : $\frac{E_{00}}{kT} \ll 1$, Thermionic Emission (TE) regime; (d): Intermediate doping : $\frac{E_{00}}{kT} \sim 1$ Thermionic Field Emission (TFE) regime.

List of Tables

Table 1: contact resistance values of W-on-Si ohmic contacts obtained with PLD and other deposition techniques after different annealing treatments.

Table 2: Barrier height values calculated in the TFE approximation of the W on Si contacts varying annealing temperature.

Table 1

Deposition method	**Annealing**			ρ_c (Ωcm^2)	**Ref.**
	Process atmosphere	Dwell time	Temp. (°C)		
PLD	N_2	5 min	200	10^{-2}	This work
PLD	N_2	5 min	450	10^{-3}	This work
PLD	N_2	5 min	850	4×10^{-4}	This work
FIB assisted deposition	--	--	--	10^{-2}	[20]
FIB assisted deposition	90% N_2, 10% H_2	15 min	450	1×10^{-4}	[20]
FIB assisted deposition	90% N_2, 10% H_2	20 min	400	1×10^{-3}	[19]
RF-Sputtering	--	--	--	$(3\text{-}6) \times 10^{-6}$	[11]
RF-Sputtering	H_2 or vacuum (10^{-7} Torr)	60 min	700	$(1.5\text{-}2) \times 10^{-6}$	[11]
CVD(*)	N_2	60 min	600	3×10^{-7}	[26]
CVD(*)	--	--	500-550	2×10^{-8}	[59]

(*) dopant concentration 10^{20} cm^{-3}

Table 2

Annealing T (°C)	ρ_c ($\Omega \cdot cm^2$)	ϕ_{Bn} (eV)
0	2.2×10^{-2}	0.48
200	1.8×10^{-2}	0.47
450	1.0×10^{-3}	0.35

Figure1
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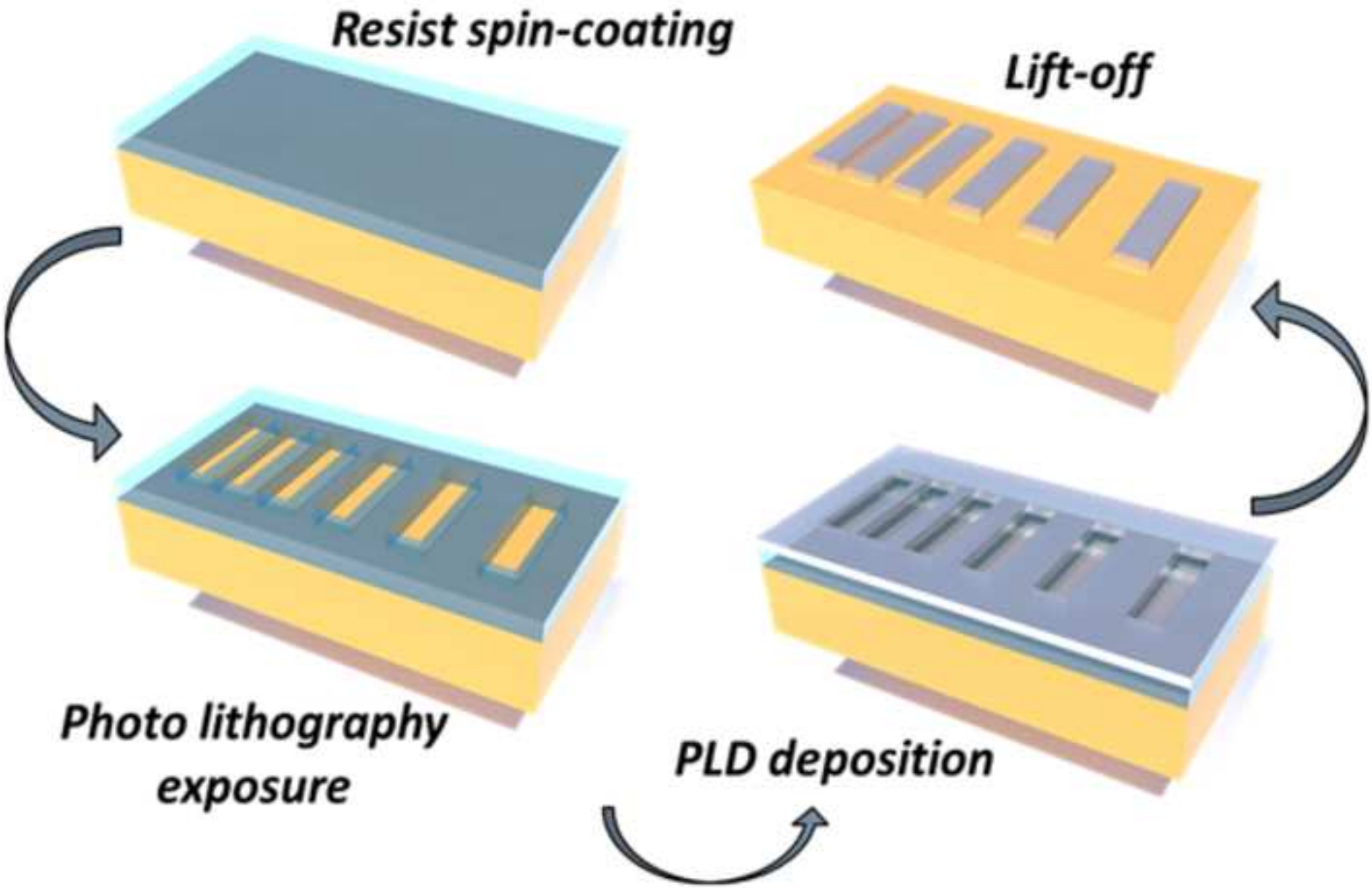

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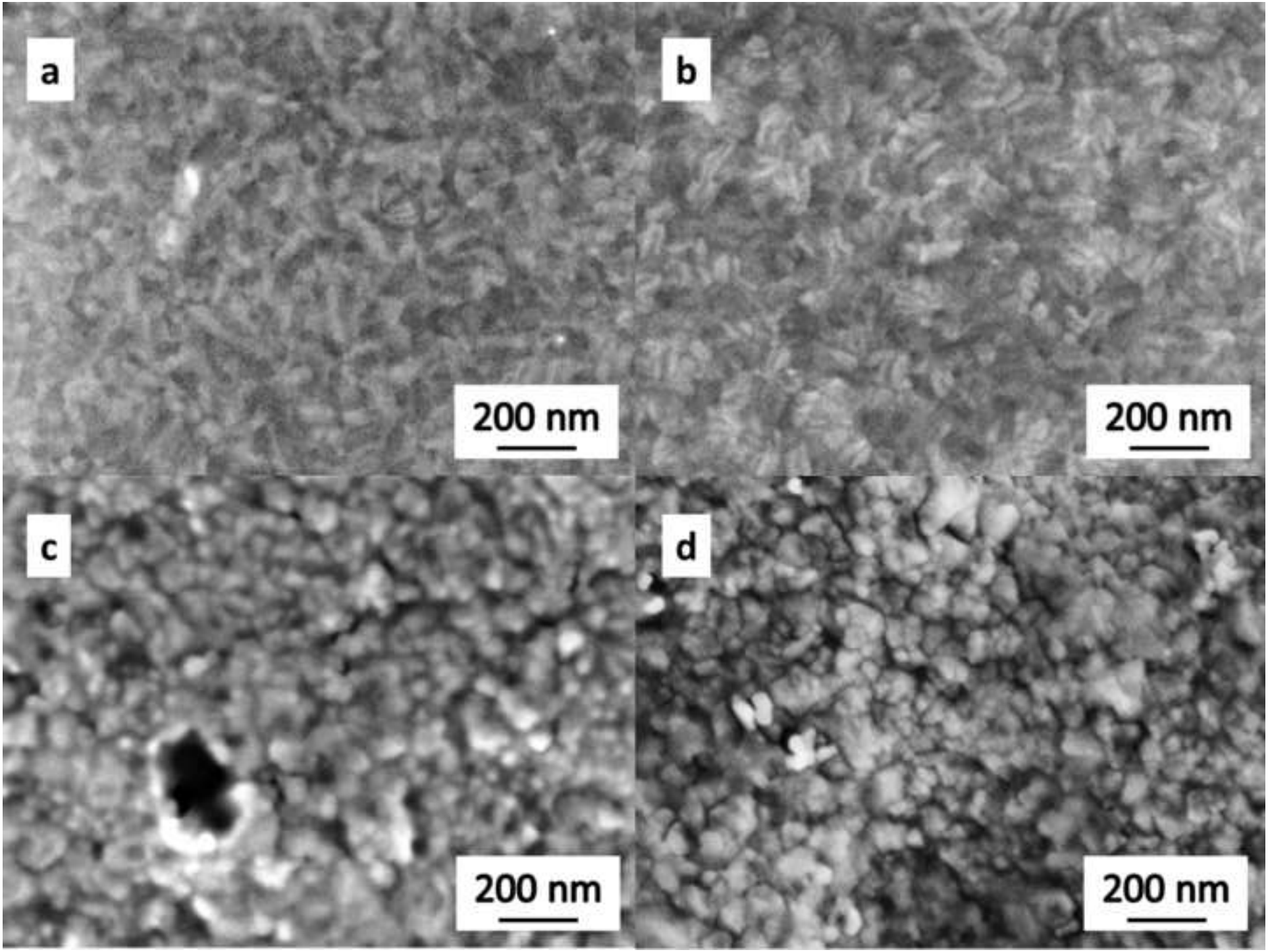

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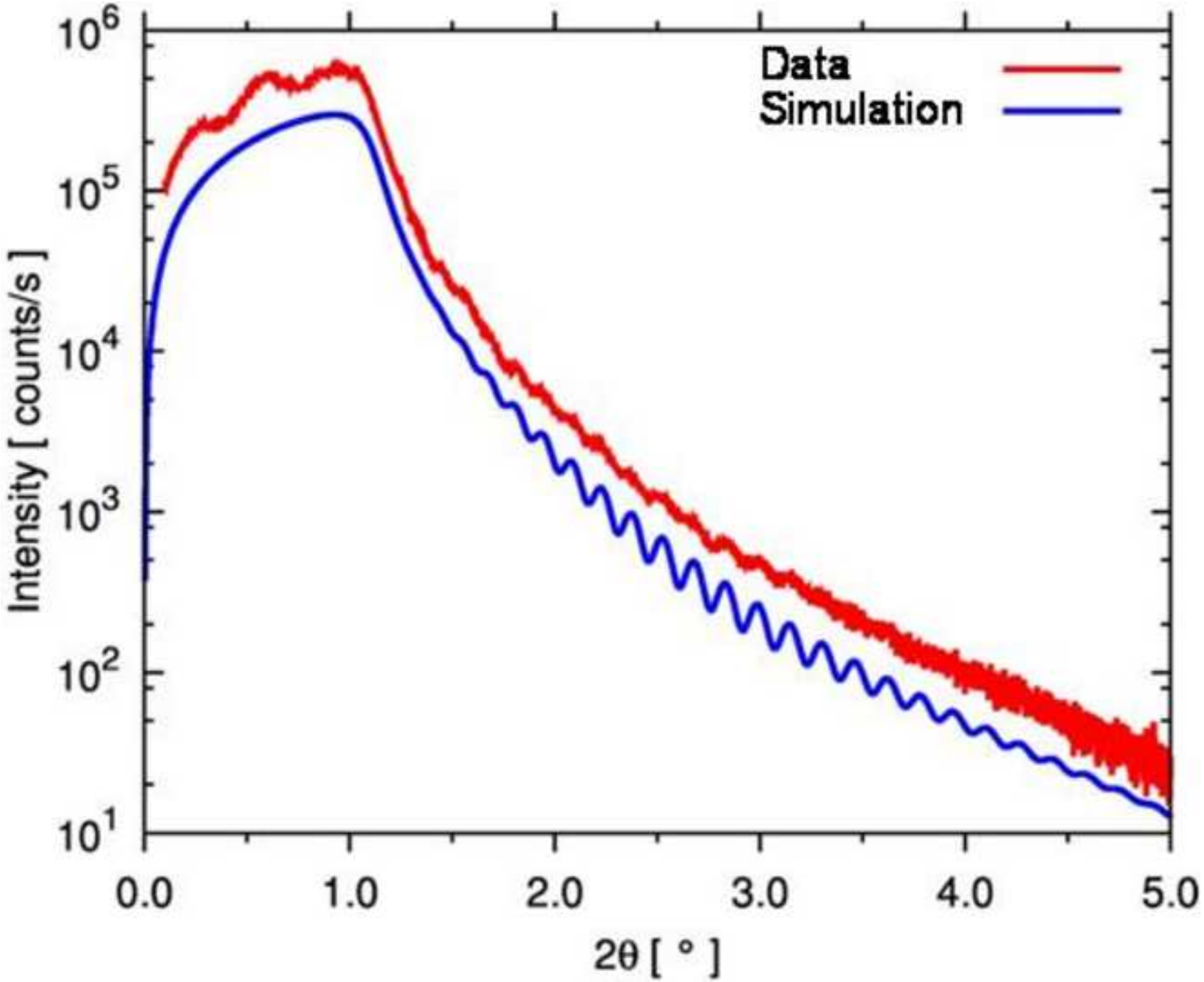

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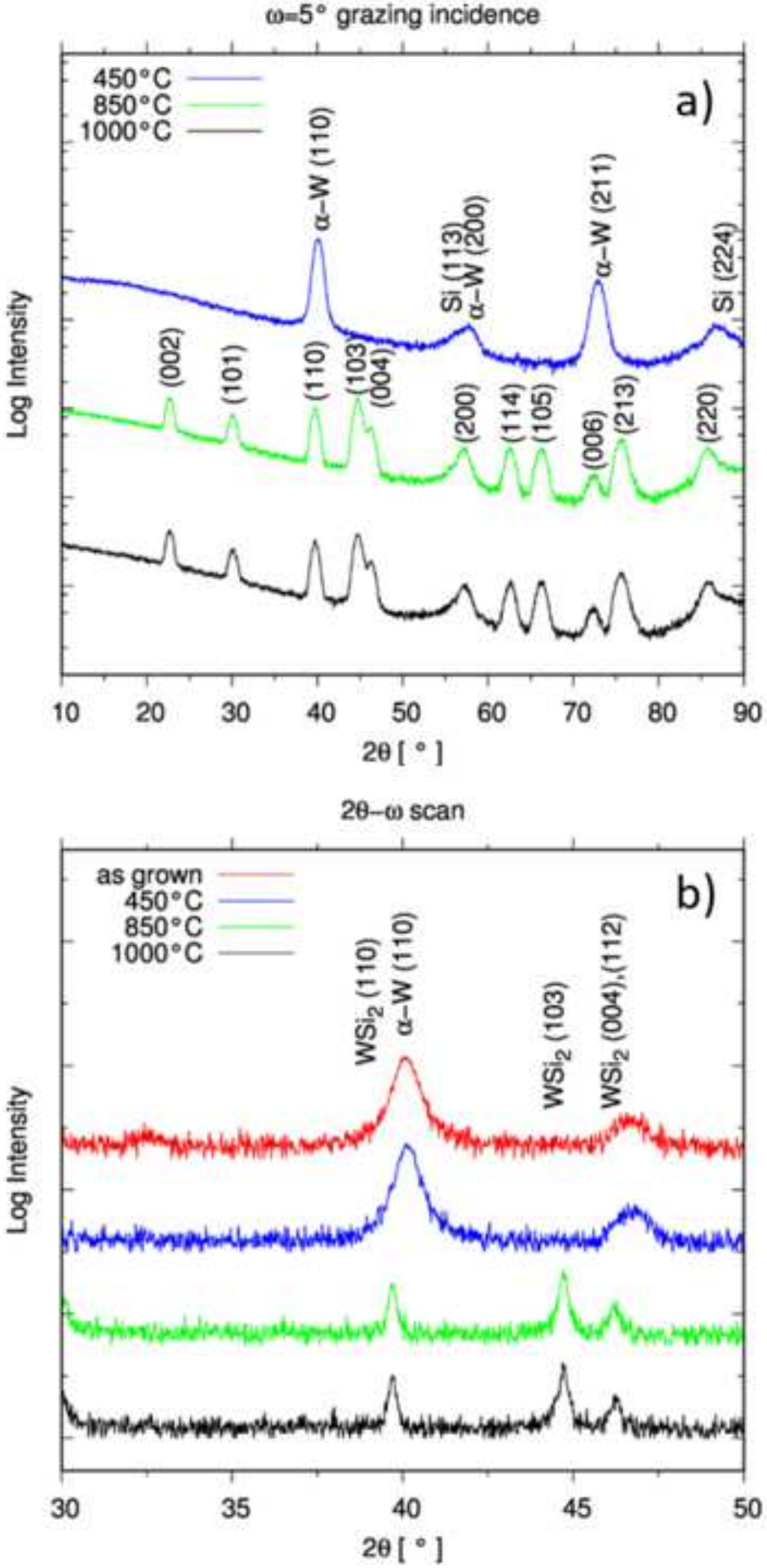

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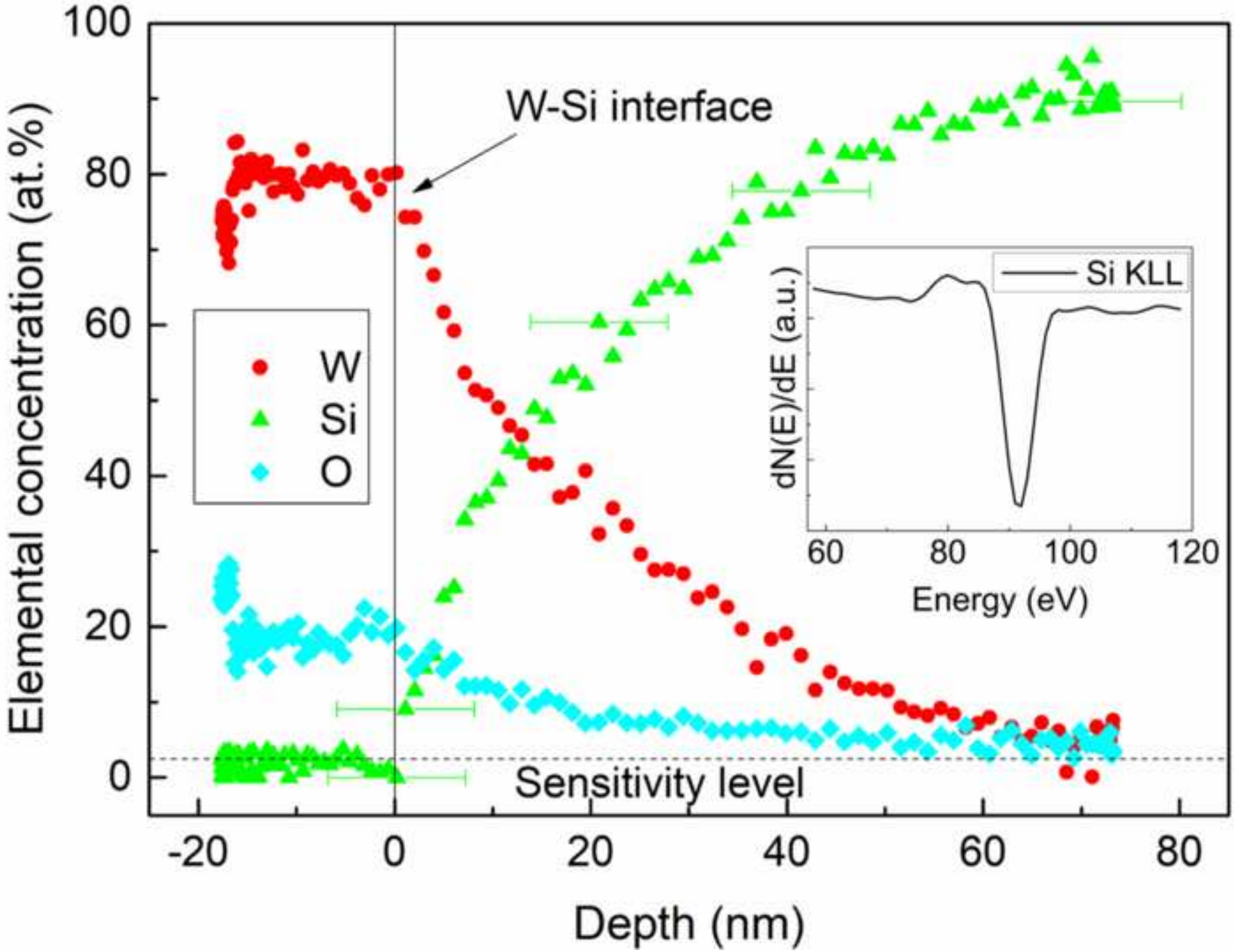

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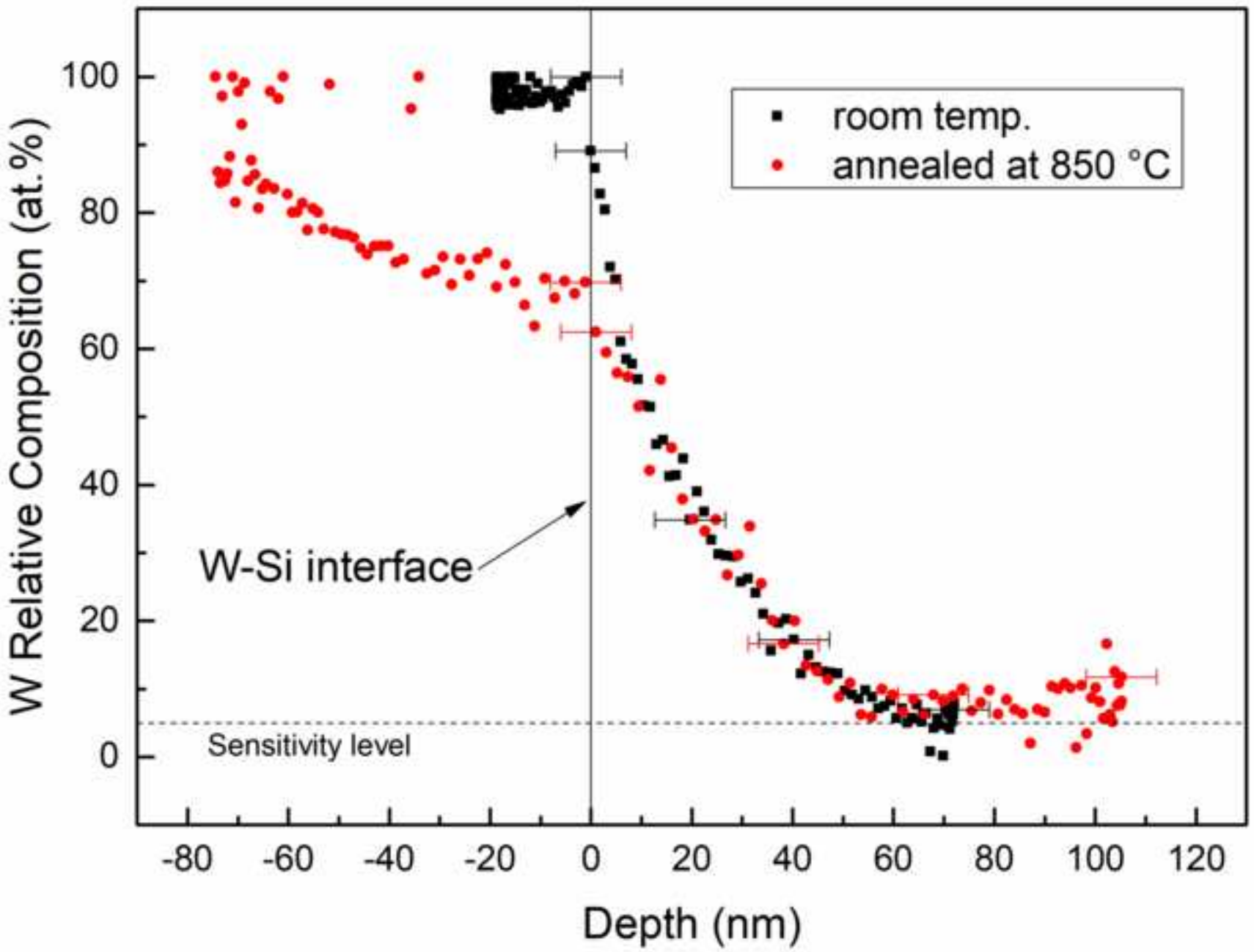

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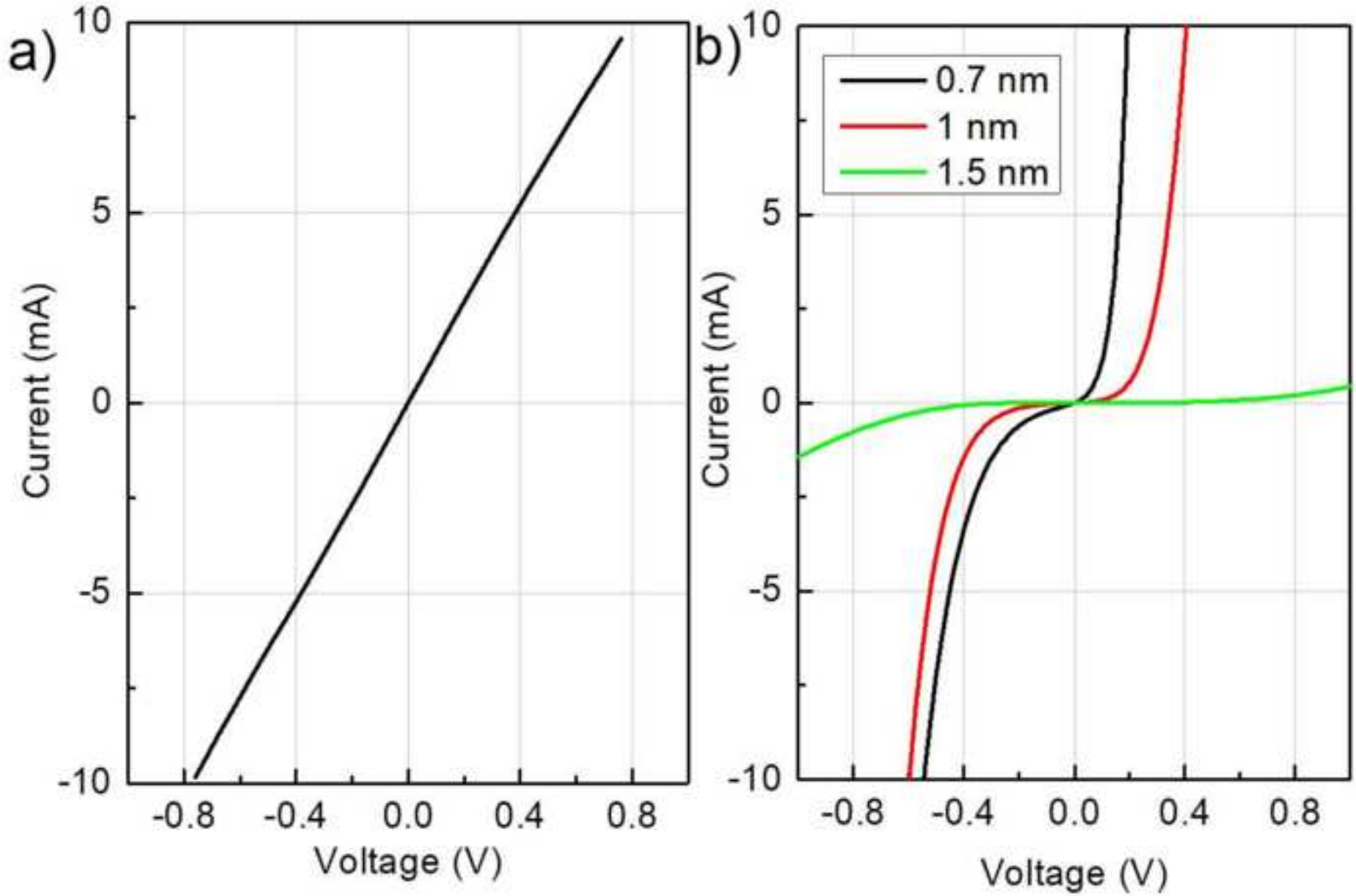

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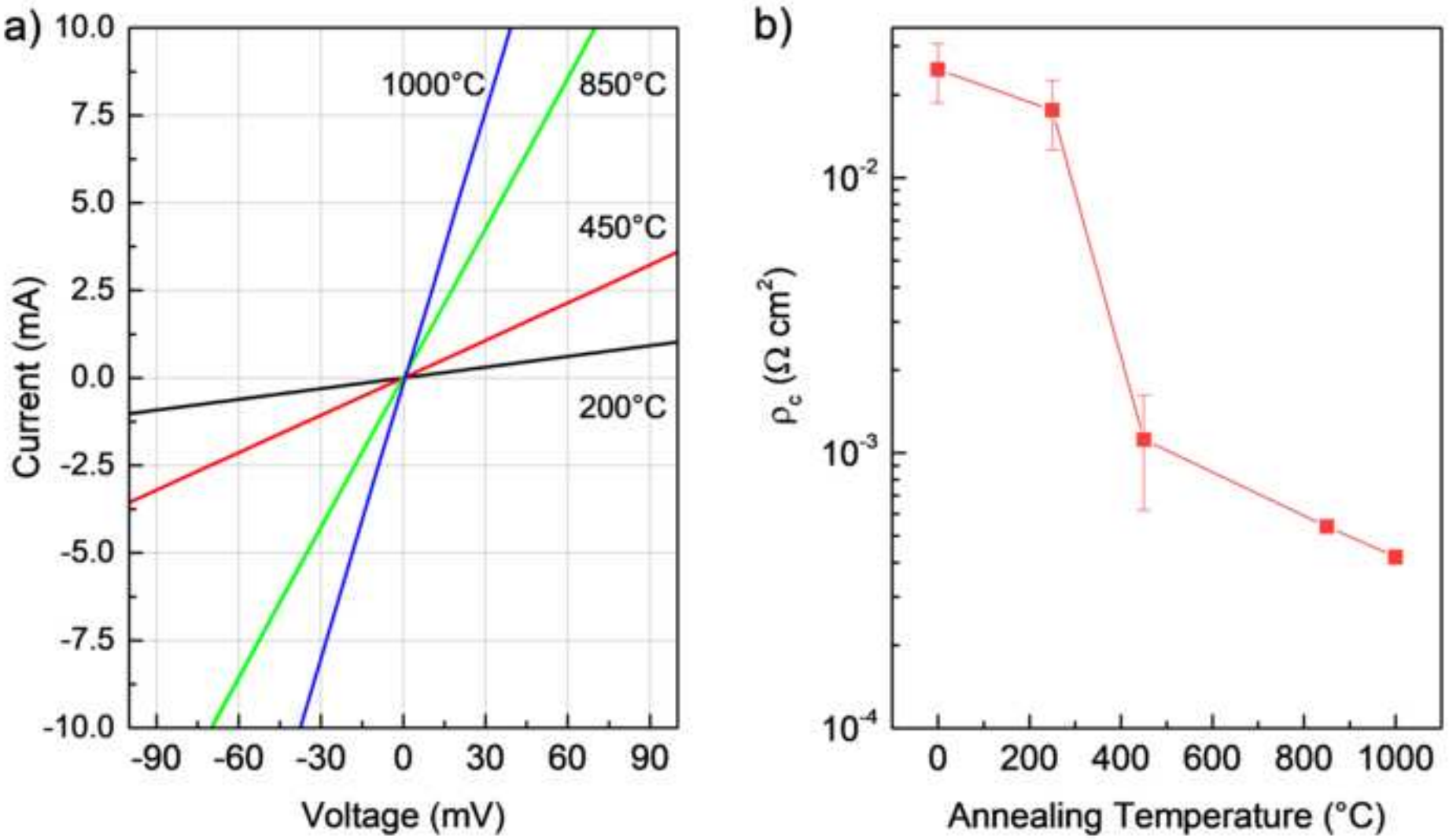

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