Miniaturized 64-channel single-photon timing system

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Abstract — **We present a portable 64-channel photon-counting system employing a monolithic array of Single-Photon Avalanche Diodes (SPADs) and a custom-designed Time-to-Digital Converter (TDC), for single-photon counting and timing applications. The system provides state-of-art single-photon detection performance and time-resolved measurement capability, with timing precision down to 100 ps FWHM and linearity better than 2% LSB (RMS). The compact form factor (1" diameter by 2" length), extensive customization capabilities, and low power consumption enable its use in applications requiring both high-end single-photon performance and system portability, such as wearable health monitoring, hand-held equipment, and automotive time-of-flight 3D ranging measurement.**

Keywords — Photon Counting; Single-Photon Avalanche Diode (SPAD); Time-to-Digital Converter (TDC); Sensor.

I. Introduction

The ability to measure fast and very faint light signals has proven to be a valuable tool in many industrial and research fields, from fluorescence decay measurement in physics, chemistry, and biology, to luminescence microscopy, diffuse optics spectroscopy, laser ranging and telemetry. Indeed, several applications, such as diffuse optical tomography (DOT) [1], fluorescence lifetime imaging (FLIM) [2], and fluorescence correlation spectroscopy (FCS) [3] require the ability of detecting light signals with sensitivity down to the single-photon level and to measure the arrival time of photons with picosecond resolution. The measurement of photon arrival times allows for the reconstruction of extremely fast periodic optic signals by means of the Time-Correlated Single-Photon Counting (TCSPC) technique [4]. This technique consists in repeatedly measuring the arrival time of single photons and building their histogram, which eventually represents the optical waveform with an equivalent analog bandwidth of hundreds of gigahertz.

To this purpose, Single-Photon Avalanche Diodes (SPADs) are widely employed in today's single-photon counting applications, offering excellent timing resolution, small size, and good photon detection efficiency in the visible and near-infrared range. Moreover, SPADs can be developed in standard CMOS technologies, enabling the monolithic integration of SPADs and electronics on the same chip. State-of-art CMOS SPADs reach performance comparable with devices developed in custom technologies in terms of timing resolution and dark counts, with the advantage of not needing off-chip circuitry to perform avalanche sensing and quenching [5].

Time interval meters for TCSPC applications have stringent requirements as well. In order to properly reconstruct optical waveforms without significant distortion, they must reach picosecond resolution and have Differential Non-Linearity (DNL) better than a few percent of the Least Significant Bit (LSB). Typically, such systems employ either a Time-to-Amplitude Converter (TAC) followed by an Analog-to-Digital Converter (ADC), or a Time-to-Digital Converter (TDC) that directly converts a time interval into a digital word. Nowadays, a typical state-of-art multichannel TCSPC system is a bulky laboratory set-up involving several single-photon detection modules and a multichannel time interval meter, able to reach up to 1 ps resolution, less than 30 ps FWHM single-shot precision, up to 12 Mcounts/s per channel and about 1% LSB (RMS) DNL [6][7]. However, such systems are not suitable for use outside of a laboratory environment, preventing their exploitation in markets such as industrial and biomedical ones, where battery powered, hand-held or even non-invasive wearable systems are a necessity. Furthermore, these instruments can only handle few (4-8) detectors in parallel, and need external routing electronics to handle more measurement channels, which negatively affects their per-channel conversion rate.

Here we present a compact and low-power, 64-channel single-photon counting system, which integrates a 32×2 SPAD array and time measurement electronics based on a TDC, able to reach an overall timing precision of 100 ps FWHM with a DNL better than 2% of the LSB (RMS).

II. System Description

The device, shown in Fig. 1, is able to operate as a complete TCSPC system with 64 detectors and a shared TDC. It is composed by two printed circuit boards housed within a very compact 1" diameter by 2" long aluminum tube, which can be easily integrated into almost any optical setup. The instrument is an evolution of the single-channel system presented in [8], with a new detector chip, frontend electronics and data processing algorithms.

The "detection board" hosts the SPAD array and two FPGAs (MAX 10, Intel Corp.) which read the detector signals. Conversely, the "time measurement board" exploits a custom-made TDC integrated circuit [9], a Spartan 6 FPGA (Xilinx

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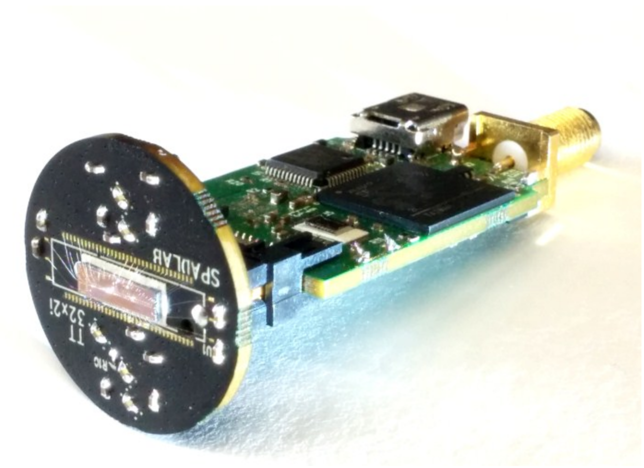

Fig. 1. Photograph of the compact TCSPC module, with detection board mounting the SPAD array chip with 32×2 pixels of 50 µm active area diameter each.

Inc.) and a high-speed USB 2.0 controller for data communication.

A. 32×2 SPAD array

The developed instrument employs a monolithic array of 32×2 SPAD detectors [10], fabricated in a standard 0.35 µm high-voltage CMOS technology, allowing for the on-chip integration of both high performance detectors and quenching circuits [11]. Two versions of the array have been manufactured: the first one having SPADs with 50 µm active area diameter and 100 µm pixel pitch (resulting in a 26% fill-factor), and the second version having 100 µm diameter SPADs with 150 µm pitch (42% fill-factor). Fig. 2 shows a microphotograph of the array chip. Thanks to the integration in each pixel of a Variable Load Quenching Circuit (VLQC) [12], the chip provides a timing output for each pixel with standard CMOS digital levels, removing the need for external readout circuitry and allowing easier interfacing to other digital circuits. Moreover, the integration of front-end electronics together with the detector allows the quenching circuit to react faster to the photon detection, thus reducing the amount of charge flowing through the SPAD. Coupled to the hold-off time enforced by the VLQC after each ignition (user-configurable from 20 ns up to tens of microseconds), this yields a greatly reduced probability of afterpulsing events.

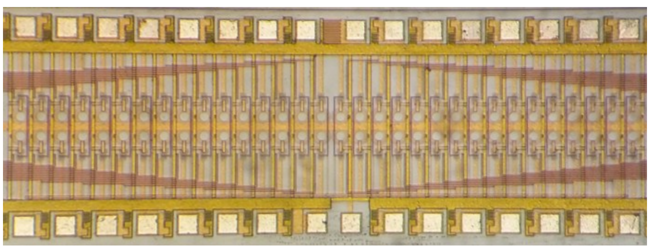

Fig. 2. Microphotograph of the 32×2 SPAD array chip. Each pixel comprises a 50 µm active area diameter SPAD and its quenching circuit. The pixel pitch is 100 µm, resulting in 26% fill-factor.

B. Detection board

In order to add programmability to the overall system, two FPGAs have been placed on the detection board itself, each one handling a 16×2 sub-array. This grants the system great flexibility of operation, as it is very easy to tailor the processing towards any specific application: from a firmware implementation with simple counters for each pixel, to pixel grouping features (e.g. combining 2x2 SPADs, for higher count rate and larger equivalent active area), to photon count windowing, and even more complicated processing algorithms. As an example, the system has been used in Speckle Contrast Optical Spectroscopy (SCOS) application, and it implements the single-shot multi-exposure speckle contrast technique described in [13], including on-board real-time processing of photon counting data and noise correction, directly providing the user with the computed speckle contrast values. This particular version of the system provided good preliminary results [14] and is currently under validation on human volunteers.

It is also possible to perform time-resolved measurements by taking advantage of the TDC hosted on the time measurement board. The easiest implementation consists in using a time-division multiplexing scheme, in order to share the single TDC present on the time measurement board between all 64 channels. The multiplexed time-to-digital conversion has been implemented following the conceptual schematic of Fig. 3. Each of the array digital outputs drives a counter (which records the real-time count-rate of the connected pixel) and is then fed to a selection circuit, which is split across both FPGAs and has been designed to avoid any triggering of spurious conversions when switching sources. The multiplexed timing information is then employed to drive the TDC front-end circuitry, while the counting information is transmitted serially to the time measurement board, which is also in charge of the multiplexing time-base generation. Of course, other different TDC sharing approaches can be easily implemented, depending on the specific application requirements.

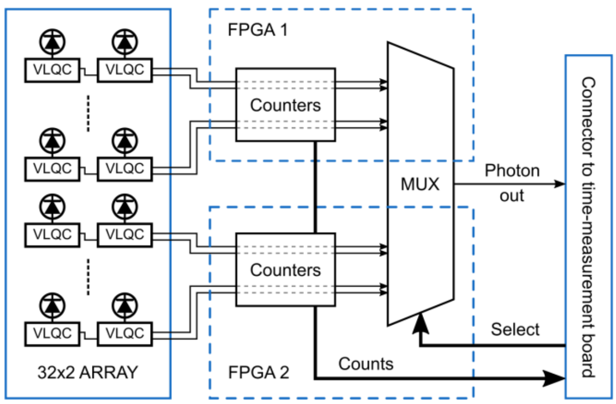

Fig. 3. Simplified block diagram of the implemented multiplexed time-to-digital conversion. Each SPAD output is connected to a counter and to a multiplexer, which is split across both FPGAs and selects the TDC input line. Count rate and selection data are streamed serially to/from the time measurement board.

C. Time measurement board

The time measurement board, described in detail in [8], hosts a custom-made TDC integrated circuit [9], which measures the time interval between a SPAD ignition and a synchronization signal (e.g. provided by an external excitation laser). The TDC is capable of 40 ps FWHM single-shot precision with 10 ps resolution, 160 ns full-scale range (FSR), and a maximum conversion rate of 5 Mconv/s. A Spartan 6 FPGA is used to manage and process data generated by the TDC, as well as to configure and communicate with the detection board and the USB 2.0 controller.

In time-resolved implementations this board generates the user-configurable TDC multiplexing time-base, and builds a histogram of photon arrival times for each channel. However, due to memory limitations of the employed FPGA, it is not possible to have 64 histograms that cover the entire measurement range with the same bin-width as the TDC (160 ns with 10 ps bin-width). The developed firmware offers the user various trade-offs to mitigate this issue. It is possible to trade between histogram bin-width and range (e.g. 2.5 ns range with a 10 ps bin, or 10 ns range with a 40 ps bin, and so on) and to select which sub-region of the TDC's FSR is to be recorded into the histogram, allowing the user to sweep the entire FSR without loss of resolution. The user can also choose to trade spatial resolution for histogram range and bin-width by grouping pixels together, essentially performing an OR of the pixel outputs, which will act as a single pixel with a larger active area.

In applications where the TDC is not needed, the Spartan 6 FPGA can be used to implement additional data processing. The measurement results are then transferred to a host PC via the USB link, which is also used to power the device.

III. Experimental Characterization

The developed module has been characterized using the 50 µm SPAD diameter version of the array. The dark count rate (DCR) for each pixel is shown in Fig. 4, with an average value of about 200 counts per second (cps) at ambient temperature and a few hot pixels (below 10%). It can be noted that the average DCR is slightly higher than the value reported in [10]; this is an effect of the increased operating temperature of the detector, caused by the power dissipation of the two FPGAs located on the small detector board.

The temporal response of the system was characterized employing a pulsed laser source (850 nm wavelength, 20 ps FWHM pulse width). For this measurement, the TDC histogram generation logic was configured to have a 20 ps bin width, resulting in a 5 ns FSR, in order to capture the full duration of the instrument response. The measurement is shown in Fig. 5 for one of the pixels, reaching a single-shot precision of 100 ps FWHM, which is mainly limited by the performance of the VLQC frontend circuit employed in the SPAD array chip. No significant differences in timing response have been observed between pixels.

The timing skew between channels has also been measured using the same optical setup as the temporal response characterization. The measurement results are reported in Figure 6, where it can be seen that the worst case skew with the current firmware is about 4.3 ns. This timing difference between channels is mostly caused by differences in signal routing inside the detection board FPGAs. It is therefore possible to characterize and compensate for channel delays after the time-to-digital conversion; the developed firmware allows for such correction, by applying an appropriate offset to each channel.

The maximum conversion rate per SPAD has been measured in the time-division multiplexing scheme. Starting with a TDC capable of 5 Mconv/s multiplexed among 64 detectors, the theoretical limit for each SPAD is about 78 kconv/s. However, due to dead times in the selection of the multiplexed pixels and some conversion losses (e.g. conversions that are in progress during a pixel switching) the system can reliably operate up to a maximum rate of 50 kconv/s per pixel. This limitation can be eased by employing smarter routing techniques according to the specific application, such as event driven multiplexing, which can lead to a better exploitation of the TDC's conversion rate.

The power consumption of the device has also been measured and is about 1 W when operating in multiplexed time-resolved mode. This value however is dependent on

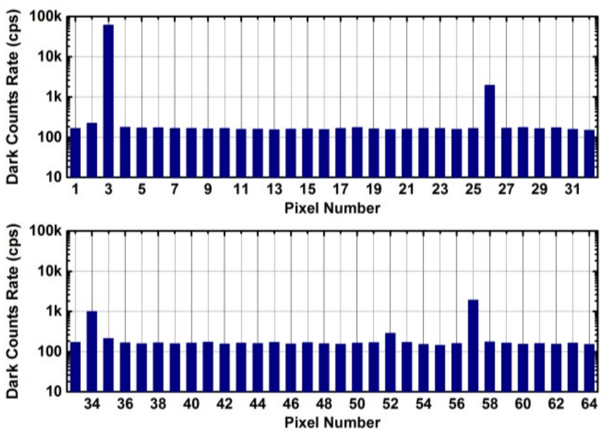

Fig. 4. Measured dark count rate of the developed system, mounting the 50 µm SPAD diameter array.

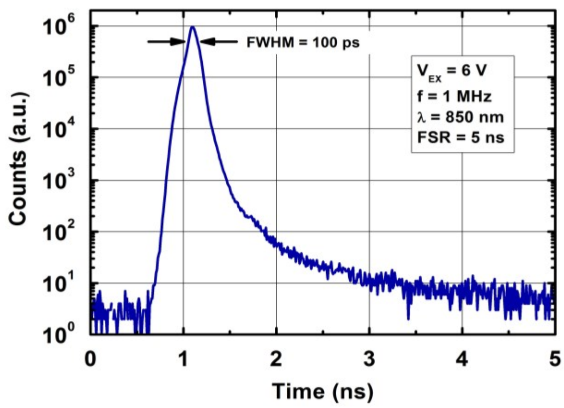

Fig. 5. Temporal response of a single pixel to a narrow (20 ps FWHM) laser pulse. The single-shot precision is 100 ps FWHM, mainly limited by the VLQC timing output.

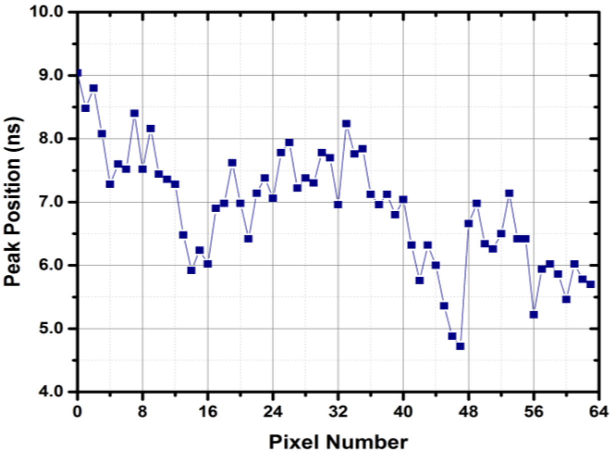

Fig. 6. Distribution of TCSPC histogram peak positions when all pixels are illuminated by a narrow laser pulse, without skew compensation.

the SPAD count rate and the amount of processing done on-board, and as such can potentially vary depending on the application-specific tailoring of the device.

IV. Conclusions

We presented a miniaturized (1” diameter by 2” long), fully configurable and customizable yet powerful time-resolved multichannel single-photon counting instrument. It includes a 64 pixel SPAD array chip (organized as two rows of 32 SPADs each) and a time measurement unit based on a custom TDC integrated circuit, capable of measuring photon arrival times with resolution down to 10 ps.

In Table 1 is reported a comparison with similar solutions presented in literature. It can be seen that this work compares favorably for those applications where portability and low power consumption are needed, while at the same time being able to provide comparable performance to bulkier and more power-hungry systems, with the main limitation of a low per-channel maximum count rate. This drawback can however be mitigated by applying a multiplexing strategy tailored for the application in which the system is deployed.

TABLE I. Comparison with similar linear SPAD arrays

Parameter	This work	[15]	[16]
No. of pixels	32 × 2	32 × 1	16 × 1
Fill Factor	26 %	15.7 %	12.5 %
DCR (80% of the pixels lower than)	200 cps	6000 cps @ T= -10°C	10000 cps
Max count rate per channel	50 kcps	1 Mcps	2.5 Mcps
Timing resolution (LSB)	10 ps	0.67 ps	10 ps
Timing accuracy (FWHM)	100 ps	63 ps	70 ps
Power consumption	1 W	70 W	3.25 W
Size	⌀ 25 mm × 50 mm	160 × 125 × 30 mm^3 plus 135 × 119 × 26 mm^3	100 × 60 × 60 mm^3

Furthermore, the system is highly programmable and readily lends itself to customization and tailoring for most specific applications. As an example, the system has been customized for use in Speckle Contrast Optical Spectroscopy (SCOS) application for investigating deep tissue blood flow [14]. The system is able to fit a 64-channel time-resolved photon counting instrument into a hand-held or wearable form factor. This opens the way for many new applications, especially in biomedical and industrial fields, which require high performance, but also portable, low power, and cost-effective instruments.

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