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# Impact of semiconducting electrodes on the electroresistance of ferroelectric tunnel junctions

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Ferroelectric tunnel junctions are promising candidates for the realization of energy-efficient digital memories and analog memcomputing devices. In this work, we investigate the impact of a semiconducting layer in series to the junction on the sign of electroresistance. To this scope, we compare tunnel junctions fabricated out of $Pt/BaTiO_3/La_{1/3}Sr_{2/3}MnO_3$ (LSMO) and $Pt/BaTiO_3/Nb:SrTiO_3$ (Nb:STO) heterostructures, displaying an opposite sign of the electroresistance. By capacitance-voltage profiling, we observe a behavior typical of Metal-Oxide-Semiconductor tunnel devices in both cases but compatible with the opposite sign of charge carriers in the semiconducting layer. While Nb:STO displays the expected n-type semiconducting character, metallic LSMO develops an interfacial p-type semiconducting layer. The different types of carriers at the semiconducting interfaces and the modulation of the depleted region by the ferroelectric charge have a deep impact on electroresistance, possibly accounting for the different sign observed in the two systems. *Published by AIP Publishing.* https://doi.org/10.1063/1.5021158

The ability of ferroelectric materials to maintain a stable state of polarization in the absence of external electric fields has found applications in many fields, such as nonvolatile memories (FeRAMs),[1] reconfigurable transistors (FeFETs),[2] electric control of magnetism,[3–5] and spintronics.[6,7] In recent years, the ability to fabricate ultrathin ferroelectric films has enabled the realization of ferroelectric tunnel junctions (FTJs), with the tunnel barrier made of a few nm-thick ferroelectric film. A sizeable resistance modulation, between high (OFF) and low (ON) impedance states, is observed upon reversal of the polarization vector **P**. The characteristic figure of merit is the so-called Tunnel Electroresistance (TER), which can be defined as $TER = \frac{(R_{down} - R_{up})}{\min(R_{down}, R_{up})}$, i.e., the variation of the resistance for **P** pointing downwards ($R_{down}$) and upwards ($R_{up}$), with reference to a planar junction, normalized to the minimum of the two resistance values.[8] Noteworthily, the viscous dynamics of ferroelectric switching allows the continuous tuning of device resistance in a memristive fashion.[9–13]

The classical explanation for the resistance change in FTJs relies on the electrostatic effects at the electrodes. In an asymmetrical FTJ, charge screening is different in the two electrodes and the ferroelectric polarization determines different band profiles whether **P** is pointing towards one or the other interface. Other mechanisms may determine the change of resistance as well,[14] such as interface effects[10,15,16] or the modulation of the Schottky-like barrier developing at the insulator-electrode interface in semiconducting electrodes.[17,18] Due to the concurrency of all these effects, predicting the magnitude or even the sign of TER can be non-trivial. A typical example is FTJs employing metallic $La_{2/3}Sr_{1/3}MnO_3$ (LSMO) as one of the electrodes, $BaTiO_3$ (BTO) as the ferroelectric barrier, and a transition metal as the other electrode. According to the electrostatic model alone, the low impedance state should correspond to **P** pointing towards the "bad metal" in the junction, i.e., LSMO. Nevertheless, most reports indicate that higher resistance is found when the ferroelectric polarization points towards LSMO,[3,4,9,12,19,20] and only some authors observe the contrary.[21–23] Recently, it has been reported that the sign of electroresistance in these heterostructures is affected by BTO termination.[16] In this letter, we discuss the crucial impact on TER of the n- or p-type character of a semiconducting layer at the electrode-barrier interface. In particular, we find that interface effects in LSMO[24–26] introduce a p-type semiconducting layer, in series to the ideal tunnel junction which can account for the TER sign in this system.

The influence of semiconducting interfaces in FTJs was investigated by Wen and coworkers,[17] showing that the modulation of the space-charge layer and associated Schottky-like barrier can provide a huge enhancement of TER. Radaelli *et al.* used Capacitance-Voltage (CV) profiling to investigate the change of capacitance upon polarization reversal in FTJs and correlate it with the barrier width modulation.[20] Here, we apply the same approach to study FTJs with n- and p-type semiconducting electrodes. First, we draft a model for the correct interpretation of complex impedance measurements in FTJs. Subsequently, we compare the results obtained from electrical measurements of Pt (5 nm)/BTO (3 nm)/LSMO (30 nm)//$SrTiO_3$(100) FTJs and analogous metal-insulator-n-type semiconductor junctions made of Pt (5 nm)/BTO (3 nm) grown on Nb-doped (0.5% wt.) $SrTiO_3$(100) (Nb:STO). The two systems show the opposite dependence of capacitance on bias, revealing the presence of a p-type semiconducting layer in Pt/BTO/LSMO. The electrostatic modulation of the depletion regions has an opposite impact on the electroresistance in Pt/BTO/LSMO and Pt/BTO/Nb:STO, thus explaining the different sign of electroresistance in the two cases. Our comparative analysis points to the major role of the modulation of space charge regions and Schottky-like barriers in FTJs, which can ultimately determine the sign of the TER and explain the apparent discrepancy between experiments and simplified electrostatic models.

To realize the FTJs, epitaxial films of BTO and LSMO were grown by pulsed laser deposition following procedures

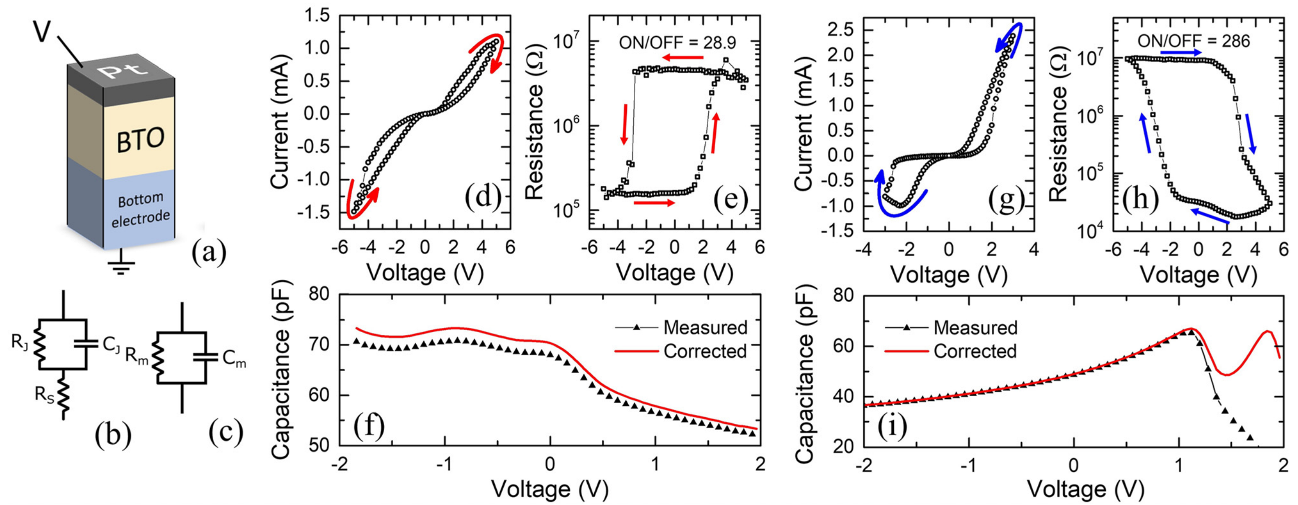


FIG. 1. (a) Device representation with indication of the electrical connections, (b) discrete component model of a FTJ, (c) equivalent circuit representation of the measured quantities. (d) IV characteristic, (e) resistance as a function of writing pulse amplitude, and (f) CV profile of a Pt/BTO/LSMO FTJ; black symbols indicate the as-measured capacitance $C_m$ and red line the corrected junction capacitance $C_J$. (g)–(i) The same as (d), (e), and (f) for Pt/BTO/Nb:STO.

reported elsewhere.[19,27] Pt top electrodes were deposited in ultrahigh vacuum ($P < 10^{-9}$ mbar) by Molecular Beam Epitaxy with a deposition rate of 1 Å/min. The growth has been carried out in a cluster tool equipped with both techniques, thus allowing the avoidance of exposure to the atmosphere.[28] After growth, 100 nm thick Ti pillars with an area of $38 \times 38\ \mu m^2$ were evaporated through a shadow mask on the sample. These pillars serve both as a hard mask for the subsequent ion-milling step needed to define the FTJs and as a thick metal pad for the electrical characterization.

Figure 1(a) is a sketch of an FTJ. The voltage is applied with probes to the top electrode, while the bottom electrode is grounded through a second device with the same area ($38 \times 38\ \mu m^2$), previously made ohmic by applying a large voltage pulse. To model the FTJ, we use a discrete component equivalent circuit as in Fig. 1(b): the junction itself is modeled with a resistor $R_J$ in parallel to a capacitance $C_J$ and the series resistance $R_S$ is also taken into account. We emphasize that the value of $R_J$ varies strongly with bias, with a pronounced nonlinear dependence on the voltage drop across the junction. The exact value of $R_S$ can be determined with a resistance measurement at high frequency $f \gg 1/(R_J C_J)$, where the junction behaves as a short circuit. Figure 1(c) presents the typical representation of the device under test in conventional impedance measurements performed with a LCR meter, including a resistance ($R_m$) and capacitance ($C_m$) in parallel.[20] The relations between measured ($C_m$, $R_m$) and actual junction parameters ($C_J$, $R_J$) can be obtained comparing the real and imaginary parts of the impedance in circuits 1(b) and 1(c)[29]

$$C_J = \frac{C_m}{(1 - R_s/R_m)^2 + \omega^2 R_s^2 C_m^2}, \quad (1)$$

$$R_J = R_m \frac{(1 - R_s/R_J)^2 + \omega^2 R_s^2 C_J^2}{(1 - R_s/R_J) - \omega^2 R_s R_J C_J^2}, \quad (2)$$

where $\omega = 2\pi f$ and $f$ is the measurement frequency.

Equations (1) and (2) show that the series resistance must be carefully considered to extract the effective junction impedance from LCR data. For $f \ll 1/(R_S C_m)$ and $R_S/R_J \ll 1$, the as-measured quantities are representative of the actual junction impedances, i.e., $R_J \approx R_m$ and $C_J \approx C_m$. However, since $R_J$ decreases rapidly with bias whereas $R_S$ remains constant, the application of high biases in CV profiling may determine large errors, even at low frequencies,[29,30] if one simply approximate $R_J$ and $C_J$ with $R_m$ and $C_m$, neglecting the effect of series impedance. Note also that, in Eqs. (1) and (2), only the real part of series impedance $R_S$ has been considered. This is a suitable approximation in the present case, where Rs models essentially the broken contact pad and parasitic capacitances can be neglected.

The above model will be used for discussing the electrical characterization of representative FTJs fabricated from Pt/BTO/LSMO (junction A) and Pt/BTO/Nb:STO (junction B) stacks, illustrated in Fig. 2. The measured values of $R_S$ are 1280 Ω (junction A) and 620 Ω (junction B). The IV characteristics of A and B are shown in Figs. 1(d) and 1(g), respectively. In both cycles, the bias voltage has been swept from 0 V to $+V_{max}$, then from $+V_{max}$ to $-V_{max}$, and finally back to 0 V in about 10 s. As expected for FTJs, we observe hysteresis in the IV curve; the opening of the loop is the typical signature of the memristive behavior associated with

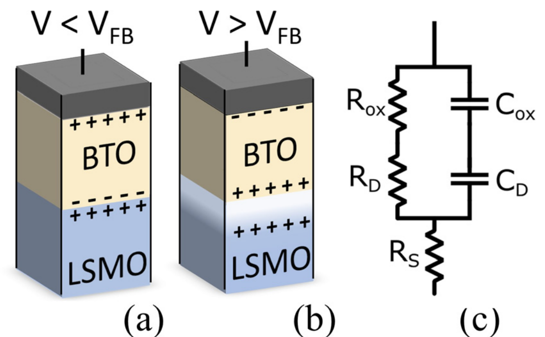


FIG. 2. (a) Sketch of a Pt/BTO/LSMO metal-insulator-semiconductor in accumulation ($V < V_{FB}$) and (b) depletion ($V > V_{FB}$). (c) Equivalent circuit accounting for the series impedance of the depleted layer. The charges in the BTO layer represent the dielectric polarization charges induced by the applied bias.

electroresistance. However, as can be seen from the arrows showing the direction of the voltage sweep, the loops are traveled in opposite directions in the two systems. In Pt/BTO/LSMO, positive voltages, which turn the ferroelectric polarization vector towards the bottom electrode ($P_{down}$), drive the system in a higher state of resistance while negative voltages (giving a $P_{up}$ ferroelectric state) determine a lower resistance. In Pt/BTO/Nb:STO, instead, the reversed dependence of resistance on polarization is found.

This difference between the two junctions is clearly visible in the resistance vs writing voltage curves presented in Figs. 1(e) and 1(h). To obtain these curves, 10 ms long pulses with amplitude ranging from −5 V to +5 V are used to write a state in the FTJ that is subsequently measured with a reading pulse of amplitude +300 mV. Clear hysteresis loops are found, with ON/OFF ratios of 28.9 for junction A and 286 for junction B, but the sign of the TER is opposite. For junction A, the OFF state is obtained for positive voltage ($P_{down}$) and the TER is positive, according to our definition, while for B the OFF state is found for negative voltage ($P_{up}$) and the TER is negative. We note that this result is coherent with previous works on Pt/BTO/LSMO[20] and Pt/BTO/Nb:STO[17,31] FTJs, and this dependence has also been recently verified in devices where the same electrodes are used with an ultrathin organic ferroelectric.[32]

Figures 1(f) and 1(i) show the capacitance of the two devices as a function of bias. For this measurement, an Agilent E4980 LCR meter has been used with a sinusoidal excitation of frequency $f = 100$ kHz and amplitude $V_{pp} = 200$ mV. At first, we prepared the junctions with a −4 V pulse lasting 100 ms and then we applied a DC bias sweep ranging from −2 V to +2 V. The as-measured capacitance $C_m$ is shown with black triangles, while the red line indicates the junction capacitance $C_J$ retrieved with Eq. (1).

Both profiles indicate a clear dependence of capacitance on bias, at variance with the constant capacitance expected for an ideal metal-insulator-metal (MIM) junction. As reported in Fig. 1(f), the capacitance $C_J$ of junction A is approximately constant for negative bias, with a value of $72.5 \pm 1$ pF, while it decreases smoothly for positive voltages. The opposite behavior is found in junction B [Fig. 1(i)], where the capacitance decreases going towards negative biases. Note that, in this case, the value of the junction capacitance for $V_{bias} > 1.2$ V is difficult to estimate. The sudden drop of $C_m$ can be misleading if no correction is applied, due to the sharp decrease of $R_J$ above 1 V of positive bias in junction B [see panel 1(g)]. As a matter of fact, the corrected value for $C_J$ [red curve in Fig. 1(i)] does not indefinitely drop for positive bias, even though it displays some spurious oscillations, essentially related to the error of the LCR meter in measuring a capacitance with a very small resistance in parallel.[29] Overall, the CV profiles of Pt/BTO/Nb:STO and Pt/BTO/LSMO junctions correspond to the ones of MIS structures with n-doped and p-doped semiconductors, respectively.[33] While for Nb:STO the n-type behavior is that expected from doping, the evidence for a p-type LSMO layer deserves some considerations. Even though the bulk metal to insulator transition in our LSMO film is found above 400 K (data not shown), the loss of metallic character at the LSMO interface can be due to the intrinsic interface effects that appear in both multilayers and free surfaces, which determine the weakening of the double exchange mechanism.[24–26] In this interfacial layer, the majority carriers are expected to be p-type, because the Sr doping introduces extra holes in $LaMnO_3$, in agreement with our CV curves. Finally, note that, at variance with Radaelli *et al.*,[20] we do not find evidence for a n-type defective BTO layer, but the different growth conditions can largely account for this difference.

Figure 2 reports a sketch useful to explain the observed CV dependence in the case of Pt/BTO/LSMO. Below the flat-band voltage $V_{FB}$, holes in LSMO are attracted towards the junction to screen negative polarization charges in BTO and the semiconducting layer results in accumulation [Fig. 2(a)]. The negative charges are related to both the ferroelectric polarization pointing upwards in the initial state, prepared with $V = -4$ V, and the dielectric polarization induced by the negative bias applied during the measurement. In this condition, the resulting capacitance is the one of the insulating oxide alone $C_{ox} = \varepsilon_0 \varepsilon_r A/d$, where A is the device area, $d$ the barrier thickness, and $\varepsilon_r$ the relative permittivity of BTO. Using the nominal geometrical parameters, a dielectric constant $\varepsilon_r = 17$ is obtained from the average value of $C_J = 72.5$ pF. The value is lower than the bulk permittivity along the tetragonal c-axis ($\varepsilon_r \sim 60$)[34] but similar to the one measured in ultrathin epitaxial films.[35] Increasing the bias, positive dielectric charges appear at the BTO/LSMO interface, partially compensating the negative ferroelectric charges and driving the semiconductor layer towards depletion [Fig. 2(b)]. The presence of the space-charge region in the bottom electrode determines both an additional series resistance $R_D$ and series capacitance $C_D$ [Fig. 2(c)]. Therefore, the device capacitance decreases according to the relation $C_J = \left(\frac{1}{C_{ox}} + \frac{1}{C_D}\right)^{-1}$. The same argument can be applied to discuss the CV profile of Pt/BTO/Nb:STO junctions, where the reversed bias dependence comes from the negative sign of majority carriers in the semiconductor. In both systems, no indication of charge inversion of the semiconductor is observed between −2 V and +2 V. As expected from the high doping concentration ($>10^{20}\,\mathrm{cm}^{-3}$), the threshold voltage lies well outside our measurement range.

We highlight that the presence of the depletion layer also impacts the shape of the IV curves. In conventional Metal-Insulator-Metal (MIM) junctions, the tunneling current can be appropriately described within the WKB approximation.[36] Instead, to include the effects of the space-charge region in MIS junctions, a more detailed and case-dependent analysis has to be undertaken.[14] This prevents any simple quantitative fitting of the IV curves at low bias, where the ferroelectric state is unaffected, unless full accumulation is reached around zero bias. As a matter of fact, Figs. 2(i) and 2(f) show that this is definitely not the case for PT/BTO/Nb:STO and to a less extent also for Pt/BTO/LSMO, because the CV curve is not flat at zero bias. Nevertheless, the effect of the additional depletion layer on the IV curves can be still qualitatively observed. A sizable rectification effect is seen in Nb:STO based FTJ [Fig. 1(g)], more notably in the high resistance state, with a larger conductance for positive bias which turns the junction into accumulation.[32] A similar effect is present in Pt/BTO/LSMO, even though it is less

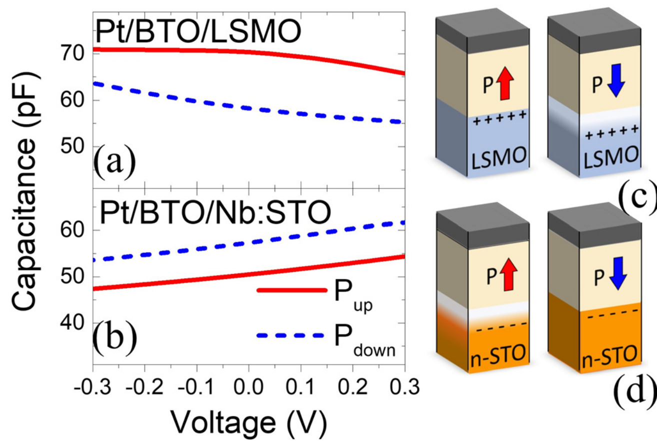


FIG. 3. (a) Junction capacitance $C_J$ as a function of bias in a Pt/BTO/LSMO FTJ after pre-polarization of the barrier in $P_{up}$ (red line) and $P_{down}$ states (dashed blue line). (b) The same for a Pt/BTO/Nb:STO FTJ. (c) Sketch representing the effect of ferroelectric polarization on the depletion layer width in Pt/BTO/LSMO and (d) Pt/BTO/Nb:STO.

evident because of the smaller depleted region associated with the larger carrier density ($N_c \sim 10^{21}\,cm^{-3}$) [Fig. 1(d)]. The rectification is still more pronounced in the high resistance state, but in this case, the high conductance is found for negative bias, where the p-type LSMO semiconducting layer is in accumulation.

The dependence of CV curves on the ferroelectric polarization is reported in Fig. 3. To obtain these measurements, we prepared the devices in the $P_{up}$ ($P_{down}$) state by applying a $-4$ V ($+4$ V) pulse (100 ms duration) and then we performed bias sweeps from $-0.3$ V to $+0.3$ V, in a range that does not affect the ferroelectric state. It clearly appears that the ferroelectric polarization has an opposite influence on the capacitance of the two devices. The negative polarization charges associated with $P_{up}$ at the bottom BTO interface reduce the depletion width in p-type LSMO based FTJs as sketched in Fig. 3(c), while they increase it in n-type Nb:STO [Fig. 3(d)]; of course, the opposite occurs for $P_{down}$. In agreement with our model, the capacitance $C_J$ of junction A [Fig. 3(a)] appears to be larger for $P_{up}$ than for $P_{down}$ and vice versa in junction B [Fig. 3(b)]. For junction B, we can estimate the change $\Delta$d of the depletion width in the different ferroelectric states. If we assume for the dielectric constant of Nb:STO $\varepsilon_r = 200$,[37] we obtain $\Delta d^{Nb:STO} = \varepsilon_0 \varepsilon_r A\left(\frac{1}{C_{down}} - \frac{1}{C_{up}}\right) = 6\,nm$, with $C_{down}$ and $C_{up}$ being the capacitances measured at $V_{bias} = 0$ in $P_{up}$ and $P_{down}$ states, respectively, and A the area of the junction. Moreover, knowing the number of donors per unit volume of Nb:STO ($N_d = 1.6 \times 10^{20}\,cm^{-3}$),[37] we can use the condition of charge neutrality to compute the variation in the surface charge density upon ferroelectric switching: $\Delta\sigma = qN_d\Delta d = 16\ \mu C/cm^2$ (q is the electron charge). This gives a reasonable value for the ferroelectric polarization of the ultrathin BTO film, about $\pm 8\ \mu C/cm^2$, confirming the soundness of our analysis. A sizeable change of the space- charge thickness can be expected in junction A as well, since the dielectric constant of doped manganites at room temperature can be well above 100, i.e., on the same order of magnitude of STO.[38,39]

Even considering the dielectric constant of bulk $LaMnO_3$ (about $\varepsilon_r = 30$ at room temperature[40]), we would still find a modulation of the space charge region of 1.1 nm.

We emphasize that the creation of the depletion region has a deep impact on the junction impedance, due to the associated Schottky-like barrier in series to the tunnel barrier.[14] The modulation of this additional barrier can act in the same direction or in competition with other mechanisms leading to TER, like the electrostatic modulation of the barrier profile. From our analysis, the high resistance (OFF) state of junctions A and B is always found for a ferroelectric polarization direction favoring the creation of a depleted region with a Schottky-like barrier, i.e., $P_{up}$ in Nb:STO and $P_{down}$ in LSMO based FTJs. In the case of LSMO, this effect appears to be dominant over the modulation of the barrier height, which should give instead an ON state for $P_{down}$. Our results indicate that the creation of an additional Schottky-like barrier in the semiconducting electrode is crucial in determining the ON-OFF states of FTJs and, in the end, the magnitude and sign of their tunnel electroresistance. This picture may also provide a complementary explanation for the high TER observed in LSMO/BTO/Nb:STO FTJs,[31] where the modulation of space charge regions associated with the p- and n-type electrodes on the two sides of the junctions adds up and amplifies the impedance modulation.

To summarize, we used impedentiometric measurements to investigate Pt/BTO/LSMO and Pt/BTO/Nb:STO FTJs with an opposite sign of the electroresistance. While the n-type semiconducting behavior is confirmed in Pt/BTO/Nb:STO, a p-type layer, possibly related to interface effects, is found in devices with LSMO bottom electrodes. The modulation of the space charge region and the associated Schottky-like barrier in the semiconducting interfacial layer can account for the opposite sign of the electroresistance in the two systems, due to the different doping of the semiconducting layers. This paper sheds light on the crucial role of interfacial semiconducting layers for the engineering of novel multilayers giving a high value of tunnel electroresistance.

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