Wavelength-Locking of Silicon Photonics Multiplexer for DML-based WDM Transmitter

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***Abstract*— We present a wavelength locking platform enabling feedback-control of silicon (Si) microring resonators (MRRs) for the realization of a 4×10 Gbit/s wavelength-division-multiplexing (WDM) transmitter. Four thermally-tunable Si MRRs are employed to multiplex the signals generated by four directly modulated lasers (DMLs) operating in the L-band, as well as to improve the quality of the DMLs signals. Feedback-control is achieved through an FPGA controller by monitoring the working point of each MRR through a transparent detector integrated inside the resonator. The feedback system provides a MRR wavelength stability of about 4 pm (0.5 GHz) with a time response of 60 ms. Bit-error rate (BER) measurements confirm the effectiveness and the robustness of the locking system to counteract sensitivity degradations due to thermal drifts, even under uncooled operation conditions for the Si chip.**

***Index Terms*— Feedback control, microring resonators, optical transmitters, photonic integrated circuits, silicon photonics, wavelength division multiplexing, wavelength locking**

I. Introduction

Feedback control has recently emerged as a key requirement to realize robust and reliable photonic integrated circuits (PICs) [1-3]. Active control is needed to steer and hold the behavior of PICs to the target working point in presence of parasitic effects such as temperature gradients, crosstalk effects, and nonlinearities. It also enables the operation of reconfigurable circuits that integrate many components and deliver complex functionalities [4-9].

For instance, in silicon (Si) photonic devices, such as microring resonators (MRRs), control issues become even more critical because of the wavelength selectivity of the MRR response and the high temperature dependence of the Si waveguides [10-15]. When managing architectures integrating many MRRs [16-18], it is challenging to identify the current resonant wavelength of each MRR in order to tune and lock their spectral response to the wavelengths of the incoming optical signals. To this aim, it is useful to have light monitors directly integrated onto the Si chip providing real-time information on the PIC status.

On a Si platform operating at wavelength around 1550 nm, integrated monitors can be realized by using for instance Ge photodetectors [19] and all-silicon waveguide detectors, the latter exploiting either sub-band-gap effects, like surface state absorption (SSA) [20-21] and defect mediated absorption induced via selective ion-implantation [22-23], or two photon absorption [24-25]. Among SSA detectors, we have recently demonstrated a transparent in-line detector, named ContactLess Integrated Photonic Probe (CLIPP) [26, 27], that does not introduce any significant perturbation on the optical field propagating in the Si waveguide. The CLIPP can be integrated inside MRRs [12, 26], thus providing direct information on the resonance condition of the MRRs,

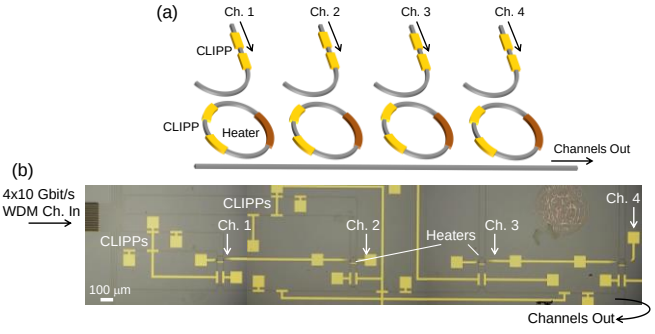

Fig. 1. (a) Schematic and (b) top-view photograph of the Si photonic WDM multiplexer. Four MRRs are coupled to a common bus waveguide to combine four input DML channels and reshape their spectrum enhancing the extinction-ratio of the transmitted signals. CLIPPs are employed as on-chip transparent detectors to monitor and lock the current working point of the circuit.

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regardless of the presence of other surrounding devices integrated on the same chip.

In this work, we demonstrate a wavelength locking platform for the control of a 4×10 Gbit/s wavelength-division-multiplexing (WDM) transmitter. As shown in Fig. 1, four Si MRRs are employed to multiplex the signals generated by four III-V-based directly-modulated-lasers (DMLs) and to operate a reshaping (carving) of each DML spectrum to improve the quality of the transmitted signal. To this aim, the resonance of each MRR is monitored through a CLIPP and locked to the emission wavelength of the related DML through a feedback control loop managed by a field-programmable-gate-array (FPGA) controller [28]. Systems like that of Fig. 1 require an extreme accuracy (<0.5 GHz) in the mutual position of the DMLs and MRRs wavelengths, and therefore offer a challenging test-bed for the proposed platform.

The paper is organized as follows. Section II discusses the design and technology of the Si photonic architecture and its operation for the multiplexing and carving of the DML signals. The wavelength locking platform employed for the control of the realized transmitter is presented in Sec. III. In Sec. IV the functionality of the locking system is demonstrated on both continuous-wave (CW) and 10 Gbit/s modulated signals. The benefits of the wavelength-locking system on the performances of the 4×10 Gbit/s WDM transmitter are shown in Sec. V. A concluding section summarizes the main results of this work.

II. Silicon Photonic Circuit

A. *Multiplexer architecture*

Figure 1(a) shows a schematic of the circuit architecture, that is composed by MRRs with independent input ports (Ch. 1 – Ch. 4) and drop ports sharing the same output bus waveguide. A top view photograph of the photonic chip, that was fabricated by the University of Glasgow, is shown in Fig. 1(b). Channel Si waveguides with 480 nm width were realized on a 220 nm silicon-on-insulator platform through e-beam lithography [29]. The MRRs have a roundtrip length of about 567 μm, resulting in a nominal free-spectral-range (*FSR*) of 125 GHz. This *FSR* is suitable to multiplex on the same output waveguide 4 signals with a spacing of 100 GHz, by tuning the MRRs resonances with 25 GHz mutual resonance shift.

The resonance wavelength ($\lambda_{R,i}$) of each MRR is individually tuned by means of a Ni-Cr heater integrated inside the resonant cavity. A CLIPP detector is integrated inside each MRR and is used as a transparent light monitor providing the feedback signal for tuning and locking operations [12]. An additional CLIPP is added at each input port, providing information on the actual optical power level of each channel coupled to the Si chip, thus making the MRR control robust against light power fluctuations (see Sec. IV). The CLIPP electrodes have size of 100 μm × 20 μm and are fabricated with the same gold layer technology of the metal strips connecting the heaters to the bonding pads [26]. Smaller size CLIPPs to be integrated into smaller resonators can be realized as described in [12, 26].

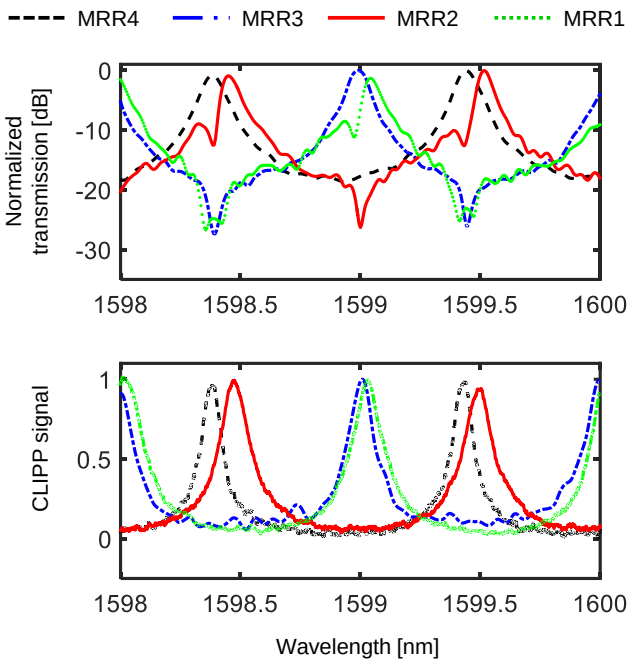

Fig. 2. Normalized drop-port spectral response of the MRRs measured (a) at the common output port of the circuit with an external conventional photodetector and (b) by the CLIPP integrated in each MRR. CLIPP monitors enable to observe the individual response of each MRR without any filtering effect [notches in (a)] originated by the through-port transmission of the cascaded MRRs.

The advantage of using CLIPP monitors for the control of the proposed architecture is shown in Fig. 2, where the wavelength-dependent drop-port transmission of the *i*-th MRR (i = 1, 2, 3, 4) is reported when all the heaters of the circuit are switched off. If the measurement is performed with a conventional photodetector coupled at the output port [Fig. 2(a)], the spectrum of each MRR is affected by the through-port transmission of the following MRRs. For instance, for the case of MRR2, two transmission notches associated with the resonances of MRR3 ($\lambda_{R,3}$= 1599 nm) and MRR4 ($\lambda_{R,4}$= 1599.43 nm) are clearly visible; in particular, the MRR4 resonance is close to the resonance of MMR2 ($\lambda_{R,4}$= 1599.5 nm), thus introducing a significant distortion of the MRR2 transmission band. By complete contrast, when CLIPPs are used to monitor the MRRs, the transmission of each microring can be decoupled from the others. For instance, Fig. 2(b) shows that a notch-free response is measured by the CLIPP integrated inside the MRRs for each transmitted channel. This enables the monitoring and control of each MRR as if it were isolated, thus reducing the complexity of the tuning and locking algorithm. In principle this concept could stand also if a conventional photodetector were integrated inside the MRR; however, the use of a conventional detector would affect the the transmitted channels as light would be tapped from the MRRs. Also, the result of Fig. 2 demonstrates the use of CLIPP detectors in the L-band, where responsivity issues emerge for conventional integrated Si-Ge photodetectors [30].

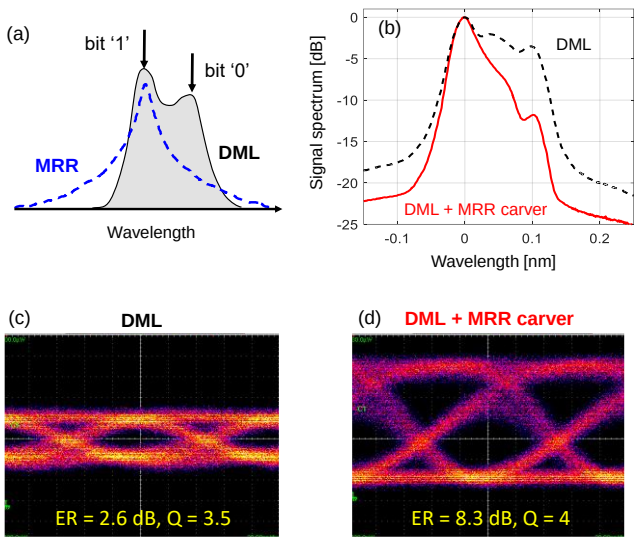

Fig. 3. (a) Schematic of the MRR carver operation: the spectrum of a DML (gray) is asymmetrically filtered by the MRR drop-port transmission; (b) Measured spectrum of a 10 Gbit/s DML before (dashed black curve) and after (red solid curve) the MRR carver. Measured eye diagram of the transmitted signal before (c) and after (d) the MRR carver, showing *ER* enhancement and Q-factor increase.

The drop-port spectrum of the MRRs has an average 3 dB transmission bandwidth of 77 pm (9 GHz), with a standard deviation of less than 2.5 pm (0.3 GHz) among the four MRRs. The off-band isolation is higher than 18 dB and the measured *FSR* is 1.05 nm (123.5 GHz). Thermal tuning efficiency of the heaters is 0.04 nm/mW, enabling wavelength tuning across an entire *FSR* with an electric power consumption of 25 mW. When tuning the MRRs wavelengths to the DMLs signals, the maximum power consumption occurs when the MRRs need to be tuned across an entire *FSR*.

B. Carver operation

In addition to the multiplexing of the four input channels (*Ch. 1 – Ch. 4*) to the common output port, each MRR is used also to reshape the spectrum of the input signal. For the application considered in this work, the *i*-th MRR is employed to enhance the extinction ratio (*ER*) between the "1" and "0" bits of a 10 Gbit/s intensity modulated data-stream generated by a DML coupled at the *i*-th input port of the circuit. To this aim, the spectrum of each DML needs to be asymmetrically filtered [28, 31-33] by suitably detuning it with respect to the MRR transmission peak, as shown in the schematic of Fig. 3(a), where the two peaks of the DML spectrum indicate respectively the "1" and "0" bits. The benefit of passing the DML signal through a filter strongly depends on the chirp behavior of the DML and on the shape of the filter [31].

Figure 3(b) shows the measured spectrum of a DML before (black dashed line) and after (red solid line) the MRR asymmetric filtering, when a 50 pm wavelength detuning is introduced between the MRR resonance and the DML spectrum. The DML, operating at a bias and a modulation current of 83 mA and 30 mA respectively, provides an output power of about 8 dBm. The carving process significantly reduces the power spectral density (PSD) associated to the '0' bits, that is located at a wavelength detuning of about 0.1 nm from the peak of the DML spectrum, where the '1' bit PSD is mainly concentrated. Figures 3(c) and (d) show the eye diagrams of the 10 Gbit/s signals, respectively measured at the output of the DML and after the MRR filter for the same input power (-8.4 dBm) at an optical sampling oscilloscope. No electrical filter has been used to measure the eye diagrams of Figs. 3(c)-(d). At the DML output the signal has a Q-factor of about 3.5 and *ER* of about 2.6 dB. After transmission through the MRR carver, the signal quality improves, reaching *ER* = 8.3 dB and a Q-factor of 4. Considering the 4 MRR multiplexer of Fig. 2 (*FSR* of 125 GHz), when the MRRs are tuned to 100 GHz spaced DMLs, the carrier wavelength of the closest concurrent DML signal is about 19 GHz (0.16 nm) from the MRR peak, where isolation is about 10 dB.

As it will be shown in the remaining of the paper, signal improvement is critically dependent on the accuracy of the detuning between the DML spectrum and the MRR resonance. Therefore, a wavelength locking platform is required to set and hold the proper positions of the MRRs resonances against thermal fluctuations or mutual thermal crosstalk effects.

III. Wavelength Locking Platform

Figure 4 shows the platform that we fabricated for the realization of a wavelength-locked 4×10 Gbit/s WDM transmitter. The structure of the transmitter is sketched in Fig. 4(a) and a photograph of the full assembly is shown in Fig. 4(b).

The 10 Gbit/s signals are generated by four III/V-based DMLs, with emission wavelength in the L-band, within 1596 nm and 1599 nm, and with 100 GHz (850 pm) mutual spacing. The DMLs were fabricated by the Fraunhofer Heinrich Hertz Institute, are packaged and have single-mode polarization-maintaining output fibers. Each packaged DML has a thermo-electric cooler (TEC) to control the temperature of the laser chip and an integrated heater to tune its wavelength. The DMLs are not stabilized though a feedback control, so that some wavelength drifts around the nominal emission wavelength may occur during operation. A radiofrequency (RF) board connects the lasers with their corresponding 10G drivers and controls the bias and modulation currents applied to each DML by means of a RF attenuator and a bias-tee.

As shown in Fig. 4(c), five fiber channels (4 polarization maintaining fibers carrying the input DMLs signals and one standard output fiber for the multiplexed channels *Ch.1 – Ch. 4*) are coupled to the Si chip performing the wavelength multiplexing and carving operations by means of a glass-based transposer manufactured by PLC Connections [34]. The transposer reduces the pitch of the fiber array in order to match the 20 μm spacing of the input/output Si waveguides. Moreover, the transposer reduces the fiber mode-field-diameter in order to match that of SU8 polymer mode adapters that are integrated on the Si chip to reduce the fiber-to-waveguide coupling loss. After packaging the transposer to the Si chip, we estimated about 5 dB loss per facet, resulting in a total output power of about -8 dBm at the locking point. Experiments reported in Figs. 3, 5 and 6 were carried out in

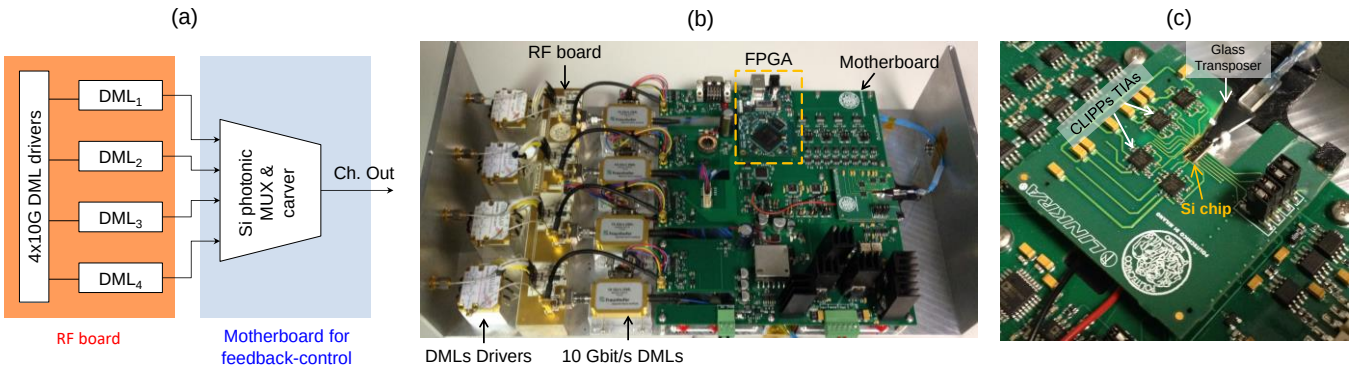

Fig. 4. (a) Schematic and (b) photograph of the 4×10 Gbit/s WDM transmitter: a RF board hosts 4 packaged DMLs and the 10 Gbit/s laser drivers, while a motherboard hosts the analog and digital circuitry for the CLIPP operation and the FPGA implementing the algorithm for tuning and locking of the Si photonic multiplexer and carver. (c) The Si chip is mounted on a PCB plugged onto the motherboard; a five-fiber array (four input fibers carrying the four DML signals to the Si photonic circuit and one output fiber for the channels output) is attached to the Si chip through a glass-based transposer.

these conditions. Subsequently, a degradation of the output power was observed because of a slight misalignment of the transposer, probably due to mechanical and thermal stress. This implied a reduction of the total power to about -20 dBm. This problem was not observed in other Si chips packaged with the same technique. However, it is worth noting that, due to the high sensitivity of the CLIPP detector, the effectiveness of the locking system is not affected by the optical power degradation observed in this sample.

The Si chip is placed onto a printed-circuit-board (PCB) [Fig. 4(c)], that hosts also the transimpedance amplifiers (TIAs) used to collect the signals of the 8 CLIPPs, according to the read-out scheme described in [26]. A TEC is placed below the Si chip to control its temperature.

The PCB hosting the Si chip is plugged into a motherboard that manages the operation of the DMLs and of the Si chip. The motherboard incorporates a microcontroller to set the bias current and the operation temperature of the DMLs, and hosts the circuitry for the generation of the sinusoidal voltage signals (digitally selectable from 1kHz to 5MHz) and for the acquisition of the CLIPP signals (amplifiers, multipliers, low pass filters, Analog-to-digital converters). The CLIPP read-out is based on a lock-in scheme allowing to balance sensitivity and response time by simply tuning the filter bandwidth.

On the motherboard there are also the drivers of the heaters of the Si chip that close the control loop on the 4 MMRs. The firmware to drive every part of the main board with digital signals and to implement the feedback control of the MRRs is resident on a FPGA (Xilinx Spartan-6) integrated on the motherboard.

IV. Wavelength Locking

According to the discussion of Sec. II.B, to achieve an *ER*-enhancement of the DML signal, the locking condition between the DML and the MRR needs to occur on the frequency slope of the MRR transmission spectrum. To this aim, two CLIPP monitors are employed, as shown in the scheme of Fig. 5(a). The first one, placed at the input port of the MRR, provides the reference signal ($CLIPP_{IN}$) giving information on the input optical power level; the second one ($CLIPP_R$) measures the optical intensity inside the MRRs, from which information on the wavelength detuning with respect to the DML spectrum can be inferred. The ratio $R = CLIPP_R/CLIPP_{IN}$ is calculated and compared to a reference value R_{set} corresponding to the desired target point, that is the MRR resonance detuning that optimizes the quality of the transmitted signal. This operation provides an error signal $\varepsilon = R_{set} - R$, which is used by an integral controller to drive the MRR heater. Depending on the sign of the error signal the heater voltage is decreased ($R_{set} < R$, cooling) or increased ($R_{set} > R$, heating).

In the next sections, wavelength locking is demonstrated when the DML operates in CW regime (Sec. IV.A) and when it is modulated at 10 Gbit/s (Sec. IV.B).

A. *Locking to a CW input signal*

To demonstrate the capability of the realized platform to lock an optical signal to a generic point of the MRR transmission slope, we consider first the case where the DML is not modulated. In this experiment, the TECs of both the Si chip and of the DML are switched on to keep stable their temperature. The case of TEC-free operation for the Si chip is discussed in Sec. IV.B.

As indicated in Fig. 5(b), we select a target locking point (red circle) at 50 pm (5.9 GHz detuning) from the resonance λ_R of the MRR, that means 5 dB below the peak transmission. We also consider that the MRR needs to be automatically tuned to the target position around the DML wavelength. The white circle of Fig. 5(b) shows the initial condition of the system, when the MRR heater is switched off and the DML wavelength is detuned by about 100 pm (11.7 GHz) with respect to λ_R, that means 10 dB below the peak transmission.

In the tuning phase, the heater voltage is progressively increased until $R = R_{set}$, that is $\varepsilon = 0$, this condition being achieved at a voltage of 1.45 V [see Fig. 5(c)-(e)]. This calibration phase is here performed in less than 100 ms. Once the target point is reached, the locking phase starts and keeps the status of the system locked around the target point ($R/R_{set} = 1$) even in presence of perturbations.

To test the effectiveness and robustness of the feedback control, we apply step-like perturbations through the MRR heater to induce both red and blue wavelength shifts of the MRR response. More specifically we induce red shifts of 35 pm (4.1 GHz), corresponding to 51% of the MRR bandwidth and inducing an output power reduction of 3.5 dB; blue-shifts

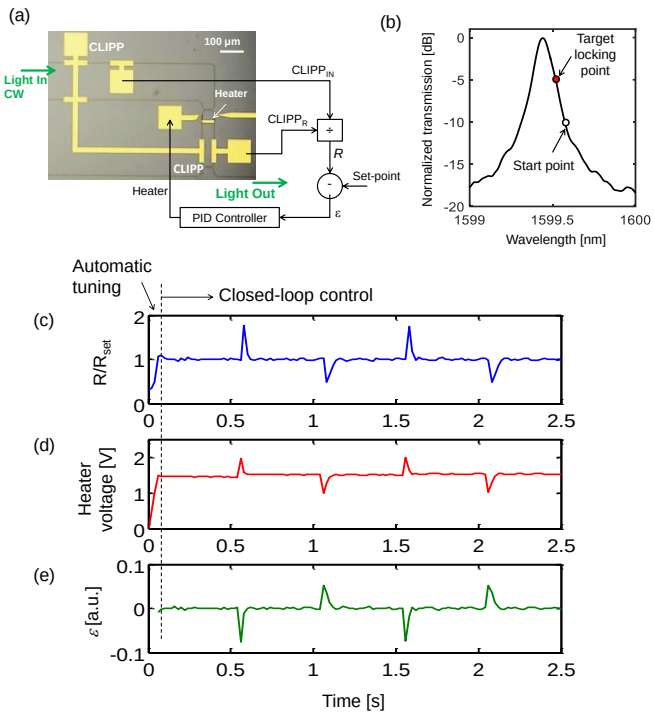

Fig. 5. Wavelength locking of the Si MRR to a CW signal. (a) Schematic of the CLIPP-assisted algorithm implemented in the wavelength locking platform. (b) Definition of the target locking point on the wavelength slope of a MRR transmission spectrum; (c) normalized ratio R/R_{set} of the CLIPP signals, (d) voltage of the MRR heater and (e) error signal measured during the tuning phase (time < 0 s) and during the locking phase (time > 0 s). In the locking phase intentional positive and negative MRR wavelength detunings are induced. In this experiment the TEC of the Si chip is switched ON.

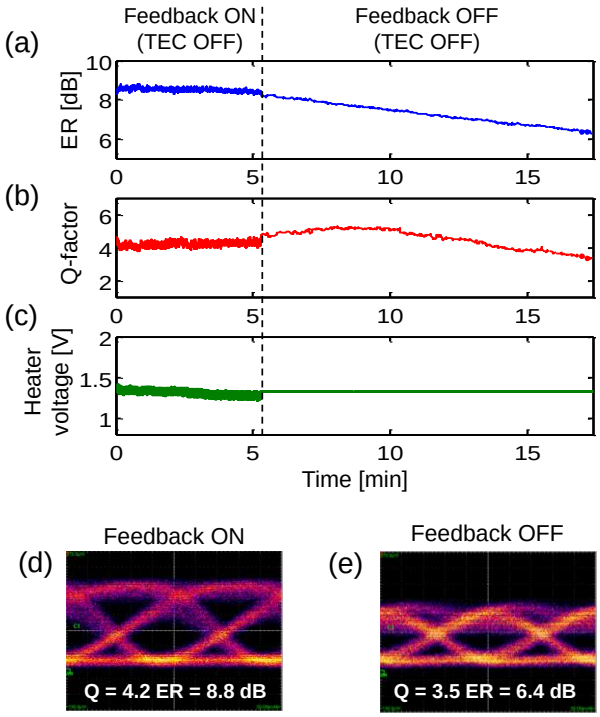

Fig. 6. Wavelength locking of a Si MRR to the 10 Gbit/s DML signal. Time evolution of the measured (a) *ER* and (b) Q of the transmitted signal when the MRR wavelength is locked to the target point (time < 5 min) and when the wavelength locking is switched off (time > 5 min). (c) Time evolution of the voltage applied to the heater of the MRR carver. Measured eye diagram of the transmitter signal when the locking system is (d) ON and (e) OFF. In this experiment the TEC of the Si chip is switched OFF.

of 21 pm (2.5 GHz), corresponding to 31% of the MRR bandwidth and inducing an output power increase of 2.5 dB. In the experiments of Fig. 5, the red-shifts are counteracted in about 60 ms and the blue-shifts in about 40 ms, this different behavior being related to the asymmetric transfer function of the MRR with respect to R_{set}. From the small residual fluctuations of R when the system is not intentionally perturbed [Fig. 5(d)], we can estimate an accuracy of the locking system here implemented of less than 0.5 GHz that, as we show in the next section, is sufficient to have a negligible effect on the *ER* of a modulated signal.

In the reported experiment, the wavelength locking is achieved with a speed of about 1 nm/s, which can compensate temperature variations as fast as 10 °C/s. This speed is sufficient to make the wavelength locking platform robust against realistic temperature changes. To further improve the speed of the closed loop control here implemented, a larger detection bandwidth of the electronic readout circuit of the CLIPP can be implemented [12]. The faster response time of the feedback system achieved in this case would come at the price of a higher noise in the electrical readout system, yet the signal-to-noise ratio can be easily maintained the same by increasing the CLIPP driving voltage. More complex control algorithms can be also employed to optimize both the locking speed and the accuracy, for instance by introducing additional digital filters whose response can be adaptively set according to the distance of the current working point from the target locking point.

It is worth noting that step-like perturbations are the worst scenario for a feedback loop system. In practical applications, laser wavelengths and MRRs resonances may drift more than a few GHz, but over a much longer time scale. The locking capture range for slow drift is only limited by the maximum temperature of the heater, that strongly depends on the employed technology. Tunability of Si MRRs is typically higher than one *FSR*. In our case this corresponds to more than 125 GHz, yet smaller MRRs with a larger *FSR* can be used to increase the capture range.

B. Locking to a 10 Gbit/s input signal

Figure 6 shows the results of the wavelength locking experiment when the signal generated by the DML is modulated at 10 Gbit/s. In particular, to test the effectiveness of the feedback system, the TEC of the Si chip is switched off. Under uncooled operation, MRRs are subject to temperature changes that are mainly due to the heating of the electronic board, and can be as large as several tens of °C degrees. In the experiments reported in the remainder of the paper, long term resonance shifts as large as one FSR are observed when the TEC is switched off. Given the temperature sensitivity of silicon channel waveguides (about 70 pm/°C at 1600 nm), this indicates that under uncooled operation the temperature of the MRRs drifts within a range of about 15 °C.

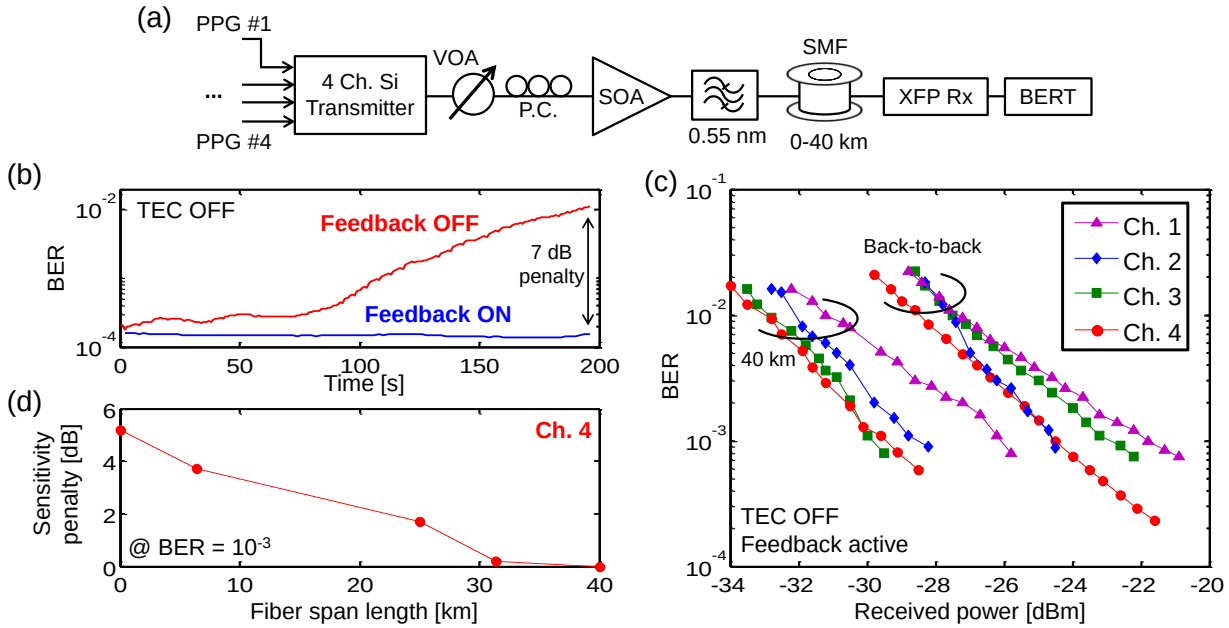

Fig. 7. (a) Schematic of the experimental setup employed for transmission experiment. (b) Time evolution of the BER measured on *Ch. 4* at the output of the transmitter when the wavelength locking is ON (blue line) and OFF (red line). Without the locking, temperature drifts degrade the BER performance by 2 decades (7 dB power penalty) on a time scale of few minutes. (c) BER curves of the four channels of the transmitter measured in back-to-back and after 40 km of SMF (feedback control of the Si chip activated, TEC of the Si chip OFF). Performance improvement is observed after fiber propagation because of the compensation of the signal pre-chirp introduced by the DMLs and the MRR carvers. (d) The reduction of the sensitivity penalty (with respect to the 40-km case) is reported in (d) for *Ch. 4* at a BER of 10^{-3} for different fiber spans from 0 to 40 km.

Figure 6(a) and (b) report respectively the time evolution of the *ER* and of the Q-factor of the DML signal transmitted through the MRR carver. In the initial point the system is set at the optimum condition shown in Fig. 3(d). When the locking system is ON (time < 5 min), the voltage applied to the heater is slightly modified by the feedback loop [Fig. 6(c)] in order to keep the MRR to the target point, thus maintaining both *ER* and Q stable around the initial values even though the TEC of the Si chip is OFF. The eye diagram of the signal transmitted through the locked MRR in this condition is shown in Fig. 6(d). The beneficial effect of the feedback is confirmed when the locking system is switched OFF, that is when the heater voltage is kept constant to a fixed value [time > 5 in Fig. 6(c)]. As the MRR wavelength undergoes the effect of temperature variations, the DML signal and the MRR start drifting apart, progressively degrading the quality of the signal. As shown in Figs. 6(a) and (b), after a time scale of only a few minutes, the *ER* drops down to less than 6.5 dB and Q-factor to about 3.5. In this condition, the aperture of the eye diagram, that is shown in Fig. 6(e), is clearly reduced.

V. Transmission Experiments

Figure 7 reports the main results of the transmission experiments performed with the wavelength-locked 4×10 Gbit/s WDM transmitter of Fig. 4. The aim of these measurements is to prove the beneficial effect of our wavelength locking platform on the quality of the transmitted channels.

The experimental setup used for BER measurements is shown in Fig. 7(a). The four L-band WDM channels generated by the Si transmitter are received one at a time by a commercial XFP receiver, and then are fed to a BER tester (BERT). External pulse pattern generators (PPGs) are employed to generate 2^{31}-1 pseudorandom bit sequences modulating the DMLs. Between the transmitter and the receiver, spools of standard single mode fiber (SMF) with increasing length from 0 km to 40 km are included. The optical power at the input of the receiver is controlled by means of a semiconductor optical amplifier (SOA) in the L-band. A filter with -3 dB bandwidth of 0.55 nm is used to reduce the optical noise contributions added by the SOA. The optical power and the polarization state of the signal at the input of the SOA are accurately controlled with a variable optical attenuator (VOA) and a polarization controller (PC).

All the measurements shown in Fig. 7 are obtained with the TEC of the Si chip switched off (as in the experiment of Fig. 6) and with the feedback control of the Si circuit activated. The closed-loop control enables to lock the operation of the Si circuit (multiplexer and carver) by fixing the spectral position of the MRR to each DML signal. The beneficial effect of the wavelength locking here implemented is shown in Fig. 7(b), where the BER of *Ch. 4* is measured as a function of time when the feedback is ON (blue line) and when is switched OFF (red line). The DML bias and modulation currents (respectively 83 mA and 30 mA peak-to-peak) provide a BER performance of about 10^{-4} at a sensitivity of -20 dBm. When the feedback is switched off, the BER performance rapidly drifts from the desired condition under the temperature fluctuations of the external environment and the thermal gradients of the electronic board. This result confirms that in this application a very accurate control of the mutual position of the DML and MRR wavelengths is needed (<0.5 GHz, i.e. a temperature control <0.05°C), and any deviation from the nominal condition results in a worse performance of the system. For example, in the case of Fig. 7(b), after only 200 s

the BER of *Ch. 4* drifts up to about 10^{-2} (red line), this variation corresponding to a 7 dB sensitivity penalty with respect to the initial condition. On the contrary, when the feedback control is active, the performance of *Ch. 4* is kept stable in time (blue line) to the desired level.

Figure 7(c) shows the BER performance of the four channels of the transmitter in back-to-back and after 40 km of SMF when the feedback control of the Si chip is activated. All the four channels have similar performance in back-to-back, with a maximum sensitivity deviation of about 2.5 dB between the best and worst channels (respectively *Ch. 4* and *Ch. 1*). The spread between the four BER curves is mainly due to slight differences in the bandwidths of the Si MRRs (9±0.3 GHz) and to the slight differences between the DML signals, although nominally identical. With reference to Fig. 1, the larger penalty of *Ch. 1* has also to be attributed to the filtering effects introduced by the through-port transmission through the following MRR2, MRR3 and MRR4. Likewise, the best performance of *Ch. 4* depends on the absence of cascaded MRRs after the multiplexing and carving performed by MRR4. Indeed, this issue can be mitigated by enlarging the free-spectral-range of the MRRs.

Even after 40 km of SMF a similar performance between the four channels is measured, with *Ch. 4* and *Ch. 1* still exhibiting respectively best and worst BER performance. Yet, it is worth noting that, after fiber propagation the performance of each channel improves. For instance, *Ch. 4* experiences a sensitivity improvement of about 7 dB at a BER of 10^{-3}. This sensitivity improvement after fiber propagation is induced by the signal chirp introduced at the transmitter and to its beneficial interaction with the fiber dispersion [33]. In particular, each MRRs introduces a normal dispersion contribution to the signals, which interacts beneficially with the anomalous dispersion of the fiber. Finally, Fig. 7(d) shows the sensitivity penalty at a BER of 10^{-3}, for different fiber spans from 0 to 40 km, with respect to the 40-km case. It is worth noting that the mutual detuning between the wavelengths of each DML and of each MRRs can be adaptively optimized to maximize the transmitter performance for different fiber spans [35].

The BER performance measured in Fig. 7 is expected to be mainly limited by two effects: first, the optical noise contributions added by the SOA used in the experiments, because of the low output power of the Si chip for this experiment (see Sec. III); second, DML lasers typically show additional thermal chirp contributions occurring on a time scale as small as few tens of ns [36]. These residual frequency excursion components, which cannot be compensated by the proposed wavelength locking system, are likely to have an impact on the overall performance of the system. This issue can be mitigated by use of a low-frequency circuit, acting on the DML bias current, carrying a low-pass-filtered copy of the incoming data to compensate for thermal chirp [31,37]. However, our results show that, if the MRRs resonances are not locked to the DML wavelengths, long-term drifts are the main impairment to the system performance.

VI. Conclusion

We demonstrated a wavelength locking platform to control a Si photonic 4×10 Gbit/s WDM transmitter with III-V-based DML signals. The transmitter integrates a Si photonic multiplexer and carver circuit, composed by four MRRs, that combines four 10 Gbit/s DML signals and enhances their *ER* ratio, from about 2.6 dB to more than 8 dB, before propagation on single-mode fiber.

The realized platform exploits CLIPP transparent monitors to lock the wavelengths of the DML input signals to the slope of the MRR spectral response, with an accuracy of better than 0.5 GHz and time response faster than 60 ms. Wavelength locking is achieved with a speed of about 1 nm/s, which is suitable to counteract temperature variations as fast as 10 °C/s High tuning speed and low power consumption (25 mW for wavelength tuning across an entire *FSR*) are the main advantages given silicon MRRs compared to wavelength locking systems based on tunable lasers and bulky etalon filters [38]. The use of CLIPP detectors integrated inside each MRR enables individual tuning and locking of the MRRs, thus making the control of the Si photonic architecture easier and more robust. The MRRs locking enables to remove the need for accurate wavelength control of the DMLs, whose emission wavelengths can be set with about 100 GHz relative spacing by simply using a TEC. Wavelength locking is also demonstrated with the TEC of the Si photonic chip switched off, proving the effectiveness of the locking system here implemented even for uncooled Si circuits.

Finally, our platform is generally applicable to manage and control other wavelength-dependent photonic integrated systems where accurate tuning and locking is required to counteract parasitic effects such as temperature gradients, crosstalk and nonlinearities. The locking algorithm must be suitably tailored according to the considered architecture and functionality of the photonic circuit, as well as on the accuracy required for the wavelength locking. For instance, if the circuit considered in this paper were used as a WDM demultiplexer at the receiver side, the MRRs peaks would have to be aligned with the signals wavelengths with no wavelength detuning, as in the example reported in [12], to minimize optical crosstalk. Moreover, optical channels should be suitably labelled, for instance trough weak modulation tones, in order to make them distinguishable by the CLIPP monitors integrated in the receiver [6, 12]. Issues related to light intensity fluctuations could be also compensated with a dithering technique, making the locking scheme independent of the light intensity [12].

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References

[1] K. Padmaraju and K. Bergman, "Resolving the thermal challenges for silicon microring resonator devices," *Nanophotonics*, vol. 3, no. 4, pp. 269–281, Aug. 2014.

[2] F. Morichetti, S. Grillanda, and A. Melloni, “Toward feedback-controlled integrated photonics,” *IEEE Photon. Jour.*, vol. 6, no. 2, pp. 1–6, Apr. 2014.

[3] Y. Li, Y. Zhang, L. Zhang, and A.W. Poon, "Silicon and hybrid silicon photonic devices for intra-datacenter applications: state of the art and perspectives," *Photon. Res.*, vol. 3, no. 5, pp. B10-B27, Jul. 2015.

[4] Z. Yu, L. Yu, F. Shaoqi, A. W. Poon, "Towards Adaptively Tuned Silicon Microring Resonators for Optical Networks-on-Chip Applications," *IEEE Jour. of Sel. Topics in Quantum Electron*, vol. 20, no. 4, pp.136-149, July-Aug. 2014.

[5] H. Jayatilleka, K. Murray, M.Á. Guillén-Torres, M. Caverley, R. Hu, N. A.F. Jaeger, L. Chrostowski, and S. Shekhar, "Wavelength tuning and stabilization of microring-based filters using silicon in-resonator photoconductive heaters," *Opt. Express*, vol. 23, no. 19, pp. 25084-25097 Sep. 2015.

[6] A. Annoni, *et al.*, “Automated Routing and Control of Silicon Photonics Switch Fabrics,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 22, no. 6, pp. 1-8, Nov.-Dec. 2016, doi: 10.1109/JSTQE.2016.2551943.

[7] P. Dong, Y. K. Chen, T. Gu, L. L. Buhl, D. T. Neilson, and J. H. Sinsky, “Reconfigurable 100Gb/s Silicon Photonic Network-on-Chip,” *J. Opt. Commun. Netw.*, vol. 7, no. 1, pp. A37–A43, Jan. 2015.

[8] J.C.C. Mak, W.D. Sacher, X. Tianyuan, J.C. Mikkelsen, Y. Zheng, J.K.S. Poon, "Automatic Resonance Alignment of High-Order Microring Filters," *IEEE J. Sel. Top. Quantum Electron*, vol. 51, no. 11, pp. 1-11, Nov. 2015.

[9] Q. Cheng, P. Stabile, A. Rohit, A. Wonfor, R. V. Penty, I. H. White, and K. A. Williams, “First demonstration of automated control and assessment of a dynamically reconfigured monolithic 8×8 wavelength-and-space switch,” *Journal of Optical Communications and Networking*, vol. 7, no. 3, pp. A388-A395, Mar. 2015.

[10] K. Padmaraju, D. F. Logan, T. Shiraishi, J. J. Ackert, A. P. Knights, and K. Bergman, “Wavelength locking and thermally stabilizing microring resonators using dithering signals,” *J. Lightw. Technol.*, vol. 32, no. 3, pp. 505–515, Feb. 2014.

[11] Y. Li and A.W. Poon, "Active resonance wavelength stabilization for silicon microring resonators with an in-resonator defect-state-absorption-based photodetector," *Opt. Express*, vol. 23, no. 1, pp. 360-372, Jan. 2015.

[12] S. Grillanda, M. Carminati, F. Morichetti, P. Ciccarella, A. Annoni, G. Ferrari, M. Strain, M. Sorel, M. Sampietro, and A. Melloni, “Non-invasive monitoring and control in silicon photonics using CMOS integrated electronics,” *Optica*, vol. 1, no. 3, pp. 129-136, Sep. 2014.

[13] J. A. Cox, A. L. Lentine, D. C. Trotter, and A. L. Starbuck, “Control of integrated micro-resonator wavelength via balanced homodyne locking,” *Opt. Express*, vol. 22, no. 9, pp. 11279–11289, May 2014.

[14] X. Zheng, E. Chang, P. Amberg, I. Shubin, J. Lexau, F. Liu, H. Thacker, S. S. Djordjevic, S. Lin, Y. Luo, J. Yao, J. H. Lee, K. Raj, R. Ho, J. E. Cunningham, and A.V. Krishnamoorthy, “A high-speed, tunable silicon photonic ring modulator integrated with ultra-efficient active wavelength control,” *Opt. Express*, vol. 22, no.10, pp. 12628–12633, May 2014.

[15] C. Li, R. Bai, A. Shafik, E. Z. Tabasy, B. Wang, G. Tang, C. Ma, C. H. Chen, Z. Peng, M. Fiorentino, R. G. Beausoleil, P. Chiang, and S. Palermo, “Silicon photonic transceiver circuits with microring resonator bias-based wavelength stabilization in 65 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1419–1436, Jun. 2014.

[16] N. Sherwood-Droz, H. Wang, L. Chen, B. G. Lee, A. Biberman, K. Bergman, and M. Lipson, “Optical 4 × 4 hitless silicon router for optical networks-on-chip (NoC),” *Opt. Express*, vol. 16, no. 20, pp. 15915–15922 Sep. 2008.

[17] L. Yang, H. Jia, Y. Zhao, and Q. Chen, “Reconfigurable nonblocking four-port optical router based on microring resonators,” *Opt. Lett*., vol. 40, no. 6, pp. 1129–1132, Mar. 2015.

[18] A. Biberman, B. G. Lee, N. Sherwood-Droz, M. Lipson, and K. Bergman, “Broadband operation of nanophotonic router for silicon photonic networks-on-chip,” *IEEE Photon. Technol. Lett*., vol. 22, no. 12, pp. 926–928, Jun. 2010.

[19] M. Pantouvaki, *et al.* "8x14Gb/s Si Ring WDM Modulator Array with Integrated Tungsten Heaters and Ge Monitor Photodetectors," in Optical Fiber Communication Conference, OSA Technical Digest (online) (Optical Society of America, 2014), paper Th1C.5.

[20] T. Baehr-Jones, M. Hochberg, and A. Scherer, “Photodetection in silicon beyond the band edge with surface states,” *Opt. Express*, vol. 16, no. 3, pp. 1659-1668, Jan. 2008.

[21] H. Chen, X. Luo, and A. W. Poon, “Cavity-enhanced photocurrent generation by 1.55 μm wavelengths linear absorption in a p-i-n diode embedded silicon microring resonator,” *Appl. Phys. Lett*, vol. 95, no. 17, pp. 171111-3, Oct. 2009.

[22] J. D. B. Bradley, P. E. Jessop, and A. P. Knights, “Silicon waveguide-integrated optical power monitor with enhanced sensitivity at 1550 nm,” *Appl. Phys. Lett*., vol. 86, no. 24, 241103-3, Jun. 2005.

[23] M. W. Geis, S. J. Spector, M. E. Grein, R. T. Schulein, J. U. Yoon, D. M. Lennon, S. Deneault, F. Gan, F. X. Kaertner, and T. M. Lyszczarz, “CMOS-compatible all-Si high-speed waveguide photodiodes with high responsivity in near-infrared communication band,” *Phot. Techn. Lett.*, vol. 19, no. 3, pp. 152-154, Feb. 2007.

[24] T. K. Liang, H. K. Tsang, I. E. Day, J. Drake, and A. P. Knights, “Silicon waveguide two-photon absorption detector at 1.5 μm wavelength for autocorrelation measurements,” *Appl. Phys. Lett.*, vol. 81, no. 7, pp. 1323-1325, Aug. 2002.

[25] T. Tanabe, H., Sumikura, H., Taniyama, A. Shinya, and M. Notomi, “All-silicon sub-Gb/s telecom detector with low dark current and high quantum efficiency on chip,” *Appl. Phys. Lett.*, vol. 96, no. 10, pp. 101103-3, Mar. 2010.

[26] F. Morichetti, S. Grillanda, M. Carminati, G. Ferrari, M. Sampietro, M.J. Strain, M Sorel, A. Melloni, “Non-Invasive On-Chip Light Observation by Contactless Waveguide Conductivity Monitoring,” *Selected Topics in Quantum Electronics, IEEE Journal of*, vol.20, no.4, pp.292,301, July-Aug. 2014

[27] F. Morichetti, *et al.*, “ContactLess Integrated Photonic Probe: Concept, Technology and Applications,” in Optical Fiber Communication Conference, OSA Technical Digest (online) (Optical Society of America, 2016), paper M2I.1.

[28] S. Grillanda, et al., "Wavelength Locking Platform for DML-based Multichannel Transmitter on a Silicon Chip," in Optical Fiber Communication Conference, OSA Technical Digest (online) (Optical Society of America, 2016), paper W1E.2.

[29] M. Gnan, S. Thoms, D. S. Macintyre, R. M. De La Rue, and M. Sorel, “Fabrication of low-loss photonic wires in silicon-on-insulator using hydrogen silsesquioxane electron-beam resist,” *Electron. Lett*., vol. 44, no. 2, pp. 115–116, Jan. 2008.

[30] D. D. Cannon, *et al.* “Tensile strained epitaxial Ge films on Si(100) substrates with potential application in L-band telecommunications,” *Appl. Phys. Lett*., vol. 84, no. 6, pp. 906-908, Feb. 2004.

[31] D. Mahgerefteh, Y. Matsui, X. Zheng and K. McCallion, "Chirp Managed Laser and Applications," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 16, no. 5, pp. 1126-1139, Sept.-Oct. 2010.

[32] N. Chimot, *et al*., "Monolithic Integration on InP of a DML and a Ring Resonator for Future Access Networks," *IEEE Phot. Techn. Lett*., vol. PP, no. 99, pp. 1-1, May 2016, doi: 10.1109/LPT.2016.2517329.

[33] P. Bernasconi et al., "DWDM Hybrid-Integrated TOSA and ROSA for 10x10.7-Gb/s Transmission Over 75-km Links," *IEEE Photonics Technology Letters*, vol. 24, no. 18, pp. 1657-1659, Sep. 2012.

[34] Transposer for multiple I/O to the Si PIC: http://www.plcconnections.com

[35] C. Ferrari, F. Morichetti, L. Flaccadori and A. Melloni, "Chromatic dispersion compensation in a ring resonator wavelength router," 2008 10th Anniversary International Conference on Transparent Optical Networks, Athens, 2008, pp. 199-202.

[36] H. Shalom, A. Zadok, M. Tur, P. J. Legg, W. D. Cornwell and I. Andonovic, "On the various time constants of wavelength changes of a DFB laser under direct modulation," IEEE J. Quantum Electron., vol. 34, no. 10, pp. 1816-1822, Oct 1998.

[37] Y. Matsui, W. Li, H. Roberts, H. Bulthuis, H. Deng, L. Lin, and C. Roxlo, "Transceiver for NG-PON2: Wavelength tunablity for burst mode TWDM and point-to-point WDM," 2016 Optical Fiber Communications Conference and Exhibition (OFC), Anaheim, CA, 2016, pp. 1-3.

[38] W. Jia, Y. Matsui, D. Mahgerefteh, I. Lyubomirsky, and C.-K. Chan, , “Generation and transmission of 10-Gbaud 0ptical 3/4-RZ-DQPSK signals using a chirp-managed DBR laser,” *J. Lightw. Technol.*, vol. 30, no. 21, pp. 3299-3305, Nov. 2012.