Design Guidelines for ContactLess Integrated Photonic Probes in Dense Photonic Circuits

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***Abstract*—The paper provides detailed guidelines for the optimal design of ContactLess Integrated Photonic Probes suitable to track and control the local optical power in photonic circuits. With reference to current technology platforms, the paper provides a guide to extract the electrical parameters of the probe and to highlight their role in defining the achievable resolution. Crucial technological and geometrical choices are discussed, together with layout and interconnection solutions oriented to a highly dense integration of the probes. Finally, the criteria for the optimal coupling of the probes to the most suitable readout electronics providing the maximization of the SNR are presented. With these guidelines in mind, transparent in-line local power monitors featuring -35 dBm sensitivity, 40 dB of dynamic range, broadband response from 1.3 to 1.6 µm, a speed down to tens of µs and a minimum size of tens of µm can be effectively designed for high performance reconfiguration and closed-loop control of complex photonic circuits.**

***Index Terms*—Silicon photonics, Optical power monitor, Non-invasive waveguide detector, Microring resonators, Photonic integrated circuits,**

I. Introduction

Photonic technologies enable today the realization of a large number of miniaturized devices on small chips with mm^2 area [1]. However, when many optical devices are integrated into complex photonic architectures, active feedback-control becomes mandatory to compensate the parasitic effects due to temperature sensitivity, crosstalk, fabrication tolerances, nonlinearities and aging [2].

The estimation of the working point of a photonic integrated circuit (PIC) is a more challenging task compared to the case of microelectronics. The main reason is that it requires the use of integrated photodetectors which absorb a certain amount of light and affect the circuit functionality [3]. This means that, targeting complex PICs with many probing points, the use of transparent photodetectors would be highly beneficial.

Recently, we have proposed a non-invasive integrated light monitor, named ContactLess Integrated Photonic Probe (CLIPP) [4]. The CLIPP measures the light intensity in a semiconductor optical waveguide through the natural generation of free carriers due to the intrinsic surface-state absorption (SSA) at the boundaries of the waveguide core [5-7]. Compared to existing SSA-based photodetectors, the non-invasive nature of the CLIPP is related to the lack of physical contacts to the waveguide core. In fact, in the case of the CLIPP, the same insulating material forming the cladding of the optical waveguide is used as dielectric between the photoconductive core and a top metal contact, thus realizing an AC-coupled detector.

The CLIPP concept has been demonstrated on both silicon (Si) [4] and indium phosphide (InP) [8] photonic platforms. Thanks to its versatility, it has been utilized in several different applications, including automatic fiber-to-waveguide alignment at a single facet [9], wavelength tuning and stabilization of micro-ring resonators (MRRs) locked both at the resonance [10] and off-resonance, for instance for carving 4×10Gb/s WDM signals generated by directly-modulated lasers [11] as well as light-path tracking and feedback-control of switch fabrics [12].

To enable the exploitation of the CLIPP in large-scale integrated photonics, the optimization of the CLIPP design becomes a crucial issue. This includes the CLIPP miniaturization, the layout on the photonic chip and the off-chip electrical interconnections to target dense photonic circuits, given the constraints of today's photonic foundries. In the following we discuss the guidelines for an optimal design of the CLIPP in Si photonic waveguides, through an in-depth analysis of its equivalent electrical circuit, systematic electrical simulations and experimental data.

The paper is organized as follows: in Sec. II we introduce the basic concepts of CLIPP detector and we briefly review the CLIPP performance achieved in previous works. In Sec. III a detailed equivalent electric circuit of the CLIPP is presented, providing the relations between the electrical and geometric parameters of the device. Sec. IV addresses issues related to the probing frequency. Guidelines for the optimization of the device layout, are given in Sec. V. Sec. VI illustrates the trade-off between speed and sensitivity, while Sec. VII focuses on the criteria for the choice of the readout electronics. A concluding section summarizes the main achievements of the paper.

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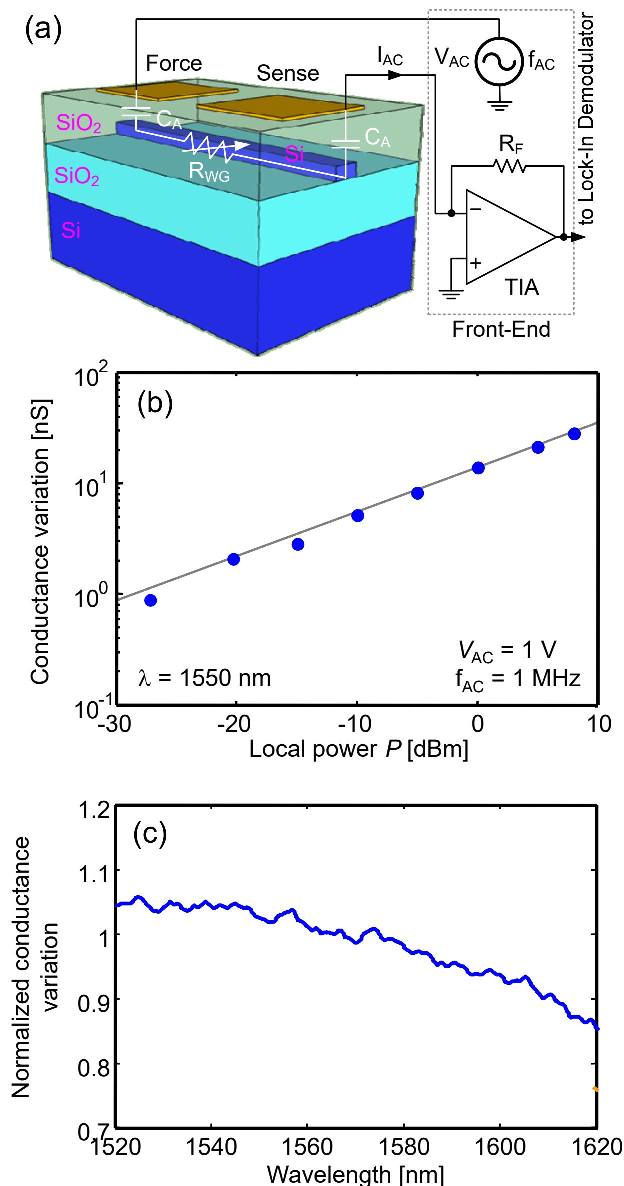

Fig. 1: (a) Scheme of the CLIPP for a Si core channel waveguide and connections to external electronics. (b) Example of CLIPP responsivity, showing the measured change of the waveguide conductance versus the optical power in the waveguide [experimental data reproduced from Ref [8]. (c) Wavelength dependence of the CLIPP signal over a range of 100 nm around 1570 nm.

II. CLIPP Concept

Figure 1(a) shows the schematic of a CLIPP integrated with a channel Si waveguide buried in a silica cladding. The CLIPP consists of two electrodes placed on top of the upper cladding, thus separated from the Si waveguide core by an electrically insulating layer. The thickness of the optically-transparent insulating layer is chosen in order to make the loss induced by the electrodes on the guided light negligible (see Sec. III).

A CLIPP sensor monitors the light intensity in the waveguide by measuring the light–induced change of the electrical conductance of the waveguide associated with SSA at the surface of the Si core [5,13]. Because the insulating layer prevents a direct DC access to the conductance of the waveguide, AC electrical probing is necessary. To this aim, an AC voltage V_{AC} at frequency f_{AC} is applied at one electrode of the CLIPP, and the current I_{AC} from the other electrode is collected by a transimpedance amplifier (TIA), feeding a lock-in amplifier for the measurement of the complex impedance between the two metallic electrodes. As will be detailed later, this impedance is related to the waveguide conductance allowing the detection of the local optical power in the waveguide. To give an example of the CLIPP responsivity, Fig. 1(b) shows the measured light-induced change of the waveguide conductance vs the optical power in a Si channel waveguide buried in a silica cladding and operating at a wavelength of 1550 nm. A sensitivity down to –30 dBm, over dynamic range of 40 dB is demonstrated [10]. In this device, the width of the Si core is w = 480 nm, and the size of the CLIPP electrodes is 20 µm × 200 µm separated by 100 µm. Previous works have proved the functionality of the CLIPP in single mode and multimode waveguides [4], both for TE and TM polarization [10]. Figure 1(c) also shows that the CLIPP exhibits a small sensitivity to wavelength, behaving as a broadband light monitor. Over a span of 100 nm around 1570 nm, an efficiency variation of ±10% is observed, that has to be attributed to a reduction of the SSA photo-generation for increasing wavelength, in agreement with decreasing photon energy. A summary of the CLIPP performances extracted from previous contributions is in Tab. I.

TABLE I
Performances of the CLIPP in Si Waveguides

Feature	Parameter	Value
Electrodes size [10]	L	100 µm
Electrodes distance [10]	D	80 – 100 µm
Minimum sensitivity [4]	P_{min}	-38 dBm
Dynamic range [4]	$P_{max}/\Delta P_{min}$	40 dB
Perturbation [4]	$\Delta n/n$	0.5 ppm
Probing voltage range [4]	V_{AC}	0.1 V - 10 V
Maximum speed *	BW	40 kHz
Operating wavelength *	λ	1.3 µm - 1.6 µm

**data referred to this work*

III. CLIPP Equivalent Electrical Model

In this section we discuss in details the equivalent electrical model of the CLIPP in order to identify the paths for the current with the aim at maximizing the current through the waveguide (modified by the local optical power) with respect to the current through all other electrical elements (not modified by the optical power). This is crucial for identifying optimization rules for the device geometry.

Figure 2 shows the main design parameters of a CLIPP integrated on a Si waveguide buried in a SiO_2 cladding. The upper and lower cladding have thickness t_{CLA} and t_{BOX}, respectively, and are taken for simplicity in this paper of the same material with relative dielectric constant ε_{ox}. The two eletrodes of the CLIPP (assumed of the same size for simplicity) have a rectangular shape, with a width W and a

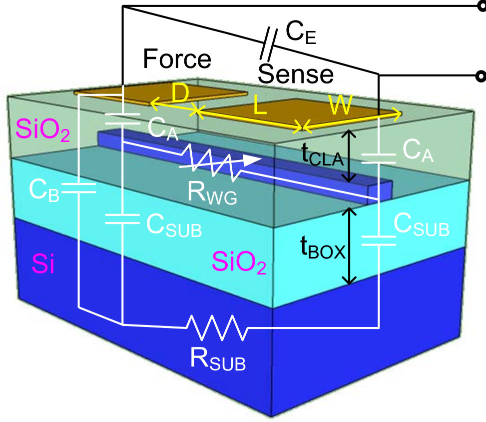

Fig. 2. Linear optical waveguide with CLIPP electrodes over the cladding highlighting the equivalent electrical model of the probe where a main sensing path from the forcing electrode to the reading electrode through the waveguide is identified (C_A-R_{WG}-C_A) in parallel to a substrate contributions (C_B-C_{SUB}-R_{SUB}). The stray capacitance (C_E) between the electrodes and the wirings connecting the probe to the front-end electronics is also highlighted.

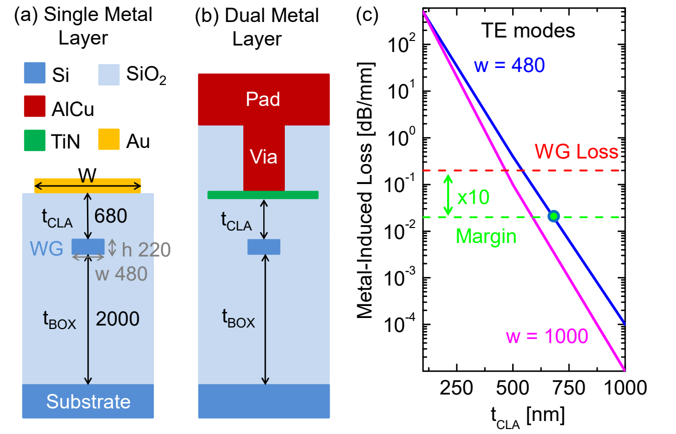

Fig. 3. Scale drawing (dimensions in nm) of two vertical cross sections of SOI technological platforms with one (a) and two (b) metal layers, where the CLIPP is implemented with a cladding thickness t_{CLA} of about 700 nm to keep negligible the metal induced loss (c) due to the CLIPP interaction with the optical field.

length L, and are separated by a distance D.

The electrical model of the structure includes the following elements:

- access capacitance C_A from the electrodes to the waveguide,
- resistance R_{WG} of the semiconductor waveguide,
- capacitance C_B between each electrode and the Si substrate,
- capacitance C_{SUB} between the waveguide and the substrate,
- resistance R_{SUB} of Si substrate,
- parassitic capacitance C_E between the CLIPP electrodes (comprising external bondings and connections).

In the following subsections, the relations between the elements of the electrical model and the design parameters of the CLIPP are extensively discussed.

A. *Waveguide resistance R_{WG} and access capacitance C_A*

The resistance R_{WG} of the Si core in the waveguide section of width w and thickness h comprised between the electrodes is given by

$$R_{WG} \cong \frac{D}{\sigma wh} \tag{1}$$

where σ is the Si electrical conductivity that changes with the number of carriers photo-generated by the optical signal in the waveguide.

The access capacitance C_A is the capacitance of the dielectric slab between the top metal electrode of width *W* and the waveguide of width *w*<<*W*. Because the electrode is much larger than the waveguide, we can estimate an effective width of ($w+2t_{CLA}$) to be used in the parallel plate expression, where the correction factor $2t_{CLA}$ accounts for the isotropic expansion of the electric fringing field [14], thus giving:

$$C_A \cong \epsilon_0\epsilon_{ox}\frac{L(w+2t_{CLA})}{t_{CLA}}. \tag{2}$$

Assuming a Si core of width *w* = 480 nm and height h = 220 nm (a common choice for single-mode Si waveguide) with an upper cladding thickness t_{CLA} = 700 nm, and a Si doping level of about 10^{15} cm^{-3}, the capacitance per unit length amounts to ~90 aF/µm (ε_{ox} = 3.9) and the resistance per unit length results ~1.3 MΩ/µm. For an electrode of L = 100 µm, C_A results ~9 fF, linearly increasing with L at the expenses of a larger area occupation of the electrode. For a distance between electrodes of 100 µm the waveguide resistance R_{WG} results equal to 130 MΩ.

From the standpoint of the AC measurement of R_{WG}, the voltage drop across C_A should be minimized by imposing its impedance, given by $1/(2\pi f_{AC}C_A)$, much smaller than R_{WG}. Consequently, a high value of C_A would be beneficial in lowering the probing frequency f_{AC} required to short this capacitance. On the other hand, the reduction of t_{CLA} causes an increase of the waveguide loss due to the light interaction with the metal electrode, as shown in the simulations reported in Fig. 3c. For a single mode waveguide (w = 480 nm) the fundamental TE mode experiences a lower loss with respect to the TM mode, due to the higher confinement of the field in the Si core. Analogously, for multimode waveguides (w = 1 µm), the higher confinement of the fundamental mode results in a slightly lower loss compared to single mode waveguides. If we target a metal induced loss 10 times lower than the intrinsic propagation loss (0.2 dB/mm, as indicated in the figure, is a common value for typical Si waveguides), we obtain a value of t_{CLA} to be around 700 nm for the effect of the CLIPP to be completely negligible independently of its size.

B. *Electrical parasitic components (C_B and C_E)*

In addition to the main path for the current signal through C_A and R_{WG} that allow to sense the resistance variation ΔR_{WG} as a consequence of local optical power variations, an alternative path for the current I_{AC} is provided through the conductive Si substrate with resistance R_{SUB} coupled by C_B. The current through this path should be minimized, i.e. its impedance should be maximized. The capacitance C_B between the top metal electrodes (dimensions W and L) and the substrate (supposed of larger area) is, similarly to Eq.(2), well described by

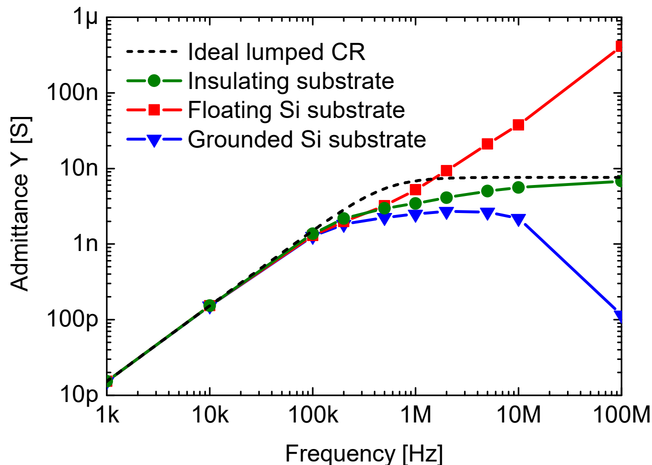

Fig. 4. FEM simulations of the CLIPP structure as in Fig.2 (L = 200 µm, D = 100 µm, W = 20 µm, C_A = 18 fF, R_{WG} = 131 MΩ, C_E = 0, t_{BOX} = 2 µm) with different electrical connections of the conductive silicon substrate, either floating or grounded. The graph shows the admittance between the two CLIPP electrodes as a function of frequency.

$$C_B \cong \epsilon_0 \epsilon_{ox} \frac{L(W + 2(t_{CLA} + t_{box}))}{(t_{CLA} + t_{box})} \tag{3}$$

where $t_{CLA} + t_{box}$ is the overall thickness of the dielectric slab. To obtain a small C_B the width W of the CLIPP electrode should be small while the length L is constrained by the choice of a sufficiently large C_A. Assuming t_{box} = 2000 nm, an electrode size of W = 5 µm and L = 100 µm, C_B results in about 13 fF. Note that a photonic platform with a bigger t_{box} is beneficial to provide smaller values of C_B.

The two CLIPP electrodes are also connected by a direct stray coupling, indicated as C_E in Fig. 2. This is due to the capacitance between the two metal electrodes and their routing to the bonding pads on the chip as well as between the corresponding bonding wires and eventually between the cables of the external connection. The capacitance C_E is driven by the same voltage signal V_{AC} of R_{WG} and produces a current that is not modulated by the optical power but is read by the same TIA. High value C_E would therefore degrade the CLIPP performance, eventually saturating the TIA itself. As the value of C_E depends primarily on the layout of the CLIPP in the photonic chip, we will recall it later in Sec. V. Despite its value, it is important to note that the current through C_E is in quadrature (up to 90° phase shifted) with respect to the signal current in R_{WG}. Thanks to this, we are solicited to use a lock-in demodulator scheme for processing the CLIPP signal to dump its effect as much as possible while selecting the signal in phase through R_{WG}.

C. Role of the substrate and its electrical connection

The Si substrate provides a resistive path, R_{SUB}, in parallel to the waveguide resistance R_{WG}. The lower the substrate resistivity, the higher is the parasitic current flowing through it that ultimately mixes with the current flowing through R_{WG}, specially at higher frequency where the admittance of C_B is lower. Low resistivity substrate therefore may lead to a reduction of the measurement sensitivity. This parallel effect on the overall current between the two CLIPP metal electrodes is shown in the Fig. 4. The dashed line corresponds to the ideal case in which only the C_A-R_{WG}-C_A path for the signal current is considered (no substrate) and their values are calculated with the lumped values given by (1) and (2), showing that the R_{WG} plateau at the expected value of about 130 MΩ is correctly reached at frequencies above 1 MHz (L = 200 µm, D = 100 µm). This ideal situation is compared in Fig. 4 with the numerical results obtained by COMSOL simulation of the full device as in Fig.2. The circles represent the simulated case in which the resistivity is made very high (insulating substrate) showing a very good matching with the lumped prediction.

The possibility to address the waveguide resistance (i.e. the plateau in the figure) in order to be sensitive to optical power variations is also verified by connecting the substrate to ground (triangles). In this case, indeed, the current signal collected by the sensing CLIPP electrode is still due to the C_A-R_{WG}–C_A path thanks to the fact that the current through the substrate is driven away by the ground short circuit. Only at very high frequencies the curve tends to decrease as a result of the current loss toward the substrate due to the distributed C_{SUB} capacitance along R_{WG}. In this situation the voltage divider given by C_A and C_{SUB} reduces the voltage across R_{WG} and correspondently decreases the plateau of the admittance spectrum.

Figure 4 also shows the detrimental effect of leaving the substrate floating (squares). In this case the device becomes a two electrodes device and consequently both currents through R_{WG} and through R_{SUB} are collected by the sensing electrode (TIA) and measured. The plateau might disappear (in fact it moves to higher frequencies the higher is the substrate doping) and the dynamic range of the TIA must be designed for a total current higher than that of R_{WG} alone.

For the best CLIPP sensitivity it is therefore important to use a high resistivity wafer and a favorable ratio between the oxide thicknesses ($t_{box} > t_{CLA}$) in order to have the overall admittance of the C_A-R_{WG}-C_A path much lower than that of the C_B-R_{SUB}-C_B path. In addition, it is important to have a solid grounding of the chip substrate. The use of suspended waveguides of micro-machined Si chips, where the bulk is etched away [15], goes favorably in the direction of a more sensitive CLIPP.

The COMSOL simulation of Fig. 4 also indicates that the capacitance C_{SUB}, which is distributed along R_{WG} toward the substrate, has a minor effect on the admittance spectrum in the frequency range of interest as long as the width W of the CLIPP electrode is larger than the waveguide width w, as it normally is.

IV. CLIPP Optimal Read-out Frequency

To highlight the interplay between the electrodes dimensions (W, L) and distance (D) and the most suitable probing frequency f_{AC}, let us take as a reference the frequency f_{low} corresponding to the pole of the admittance of the C_A-R_{WG}-C_A path when the substrate effect is negligible,

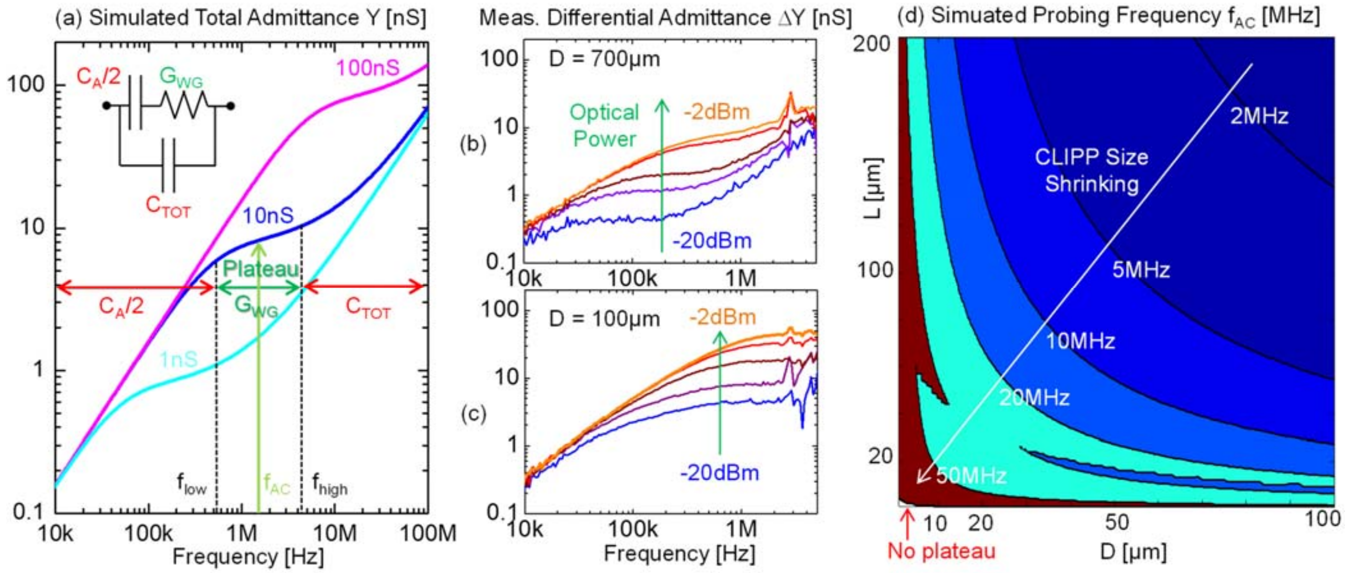

Fig. 5. (a) Simulated CLIPP admittance spectra Y approximated with the lumped model in the inset (with G_{WG} = 1, 10 and 100 nS, C_A= 18 fF, C_{TOT} = 1 fF), showing the shift of the plateau as G_{WG} varies. (b) (c) Shift of the plateau in the measured differential admittance spectra for two values of D (700 vs 100 µm, L = 200 µm, grounded substrate) for increasing local optical power (-20, -15, -10, -5, -2 dBm). (d) Simulation of the interplay between the CLIPP footprint (L, D) and the corresponding probing frequency f_{AC}. CLIPP miniaturization results in higher f_{AC}; at 50 MHz the minimum CLIPP length is 50 µm (L = 20,D = 10 µm).

corresponding to the lower bound of the sensing plateau as discussed in Fig. 4:

$$f_{low} = \frac{1}{2\pi R_{WG} C_A/2} \sim \frac{1}{DL}\,. \qquad (4)$$

In order to measure the resistance $R_{WG} = 1/G_{WG}$ without the attenuation caused by the voltage drop across C_A (i.e. well in the resistive plateau), the CLIPP operating frequency f_{AC} should be higher than f_{low}. Note that a reduction in size of the CLIPP, i.e. D and L, implies increasing f_{AC}. Assuming the coupling to the waveguide and its resistance only proportional to the length of the electrode L and the distance between the electrodes D respectively, given a certain total CLIPP length (LT), the lowest operating frequency is obtained with L=LT/4 and D=LT/2. Figure 5 (a) reports the admittance spectra simulated using the simplified electrical model shown in the inset, where C_{TOT} is the total capacitance in parallel to the main sensing path C_A-R_{WG}-C_A. In the common situation of $R_{SUB} \ll R_{WG}$, C_{TOT} is given by C_B (CLIPP device) in parallel to C_E (external connection). The simulations are reported for three values of conductivity of the waveguide, i.e. for different local optical power, and show the existence of a range of frequencies where the admittance is sensitive to R_{WG}. Figures 5 (b) and (c) report the differential admittance spectra ΔY obtained subtracting the spectrum recorded in absence of light from the spectrum measured as a function of local optical power (from -20 dBm to -2 dBm) for two values of D (100 and 700 µm). A differential measurement is preferred to reduce the admittance term given by C_{TOT}, ideally independent of the optical power. The figures show i) how the admittance increases with light intensity, ii) how the plateau shifts to higher frequency for increasingly smaller CLIPPs (shorter D) in accordance to (4) and iii) how the plateau shifts to higher frequency also when increasing the optical power, i.e. the conductivity of the waveguide increases and the resistance R_{WG} decreases. Thanks to the sub-linear relation between conductivity and optical power [4], a span of about two orders of magnitude of optical power corresponds to only one decade of variation of the value of G_{WG} and, correspondingly of f_{low} (since C_A is fixed), thus allowing operation at a fixed frequency f_{AC}, as exemplified by the arrow in Fig. 5(b) and (c). In case extremely large dynamic ranges (>30 dB) should be monitored, an adaptive algorithm for tracking the conductance by adjusting f_{AC} would represent a feasible and robust solution.

Since f_{low} is inversely proportional to the product D·L, a size reduction of the CLIPP (as might be the case when fitting the CLIPP into small ring resonators) corresponds to an increase of f_{low} and consequently of the operating frequency f_{AC}. As visible in Fig. 5(a-b), an increase of f_{AC} collides with f_{high}, the upper bound of the plateau due to C_{TOT}: $f_{high} \sim 1/(2\pi \cdot R_{WG} \cdot C_{TOT})$. The contour plot of Fig. 5d shows the value of the optimal f_{AC} as a function of L and D. In this numerical simulation, C_{TOT} includes C_B and the direct coupling capacitance between the two coplanar electrodes through air and silicon, estimated with conformal mapping expressions [16]. In this map, if the plateau extends for more than a decade, f_{AC} is set as $10 \cdot f_{low}$. If the plateau is narrower, f_{AC} is the mean between f_{high} and f_{low}. Finally, if $f_{high} \leq f_{low}$, the plateau vanishes. This plot can be useful in sizing the optimal CLIPP dimension. Although in its prototypal implementation, the CLIPP operation was initially demonstrated with conservative values (L = 2D = 200 µm), a significant reduction of this size can be achieved. In fact, setting, for instance, L = 2D = 20 µm (L_{TOT} = 50 µm, compatible with the size of most photonic devices) would require f_{AC} around 50 MHz.

Going high in measurement frequency requires a careful pace. In order to extend f_{AC} to such high frequencies, the

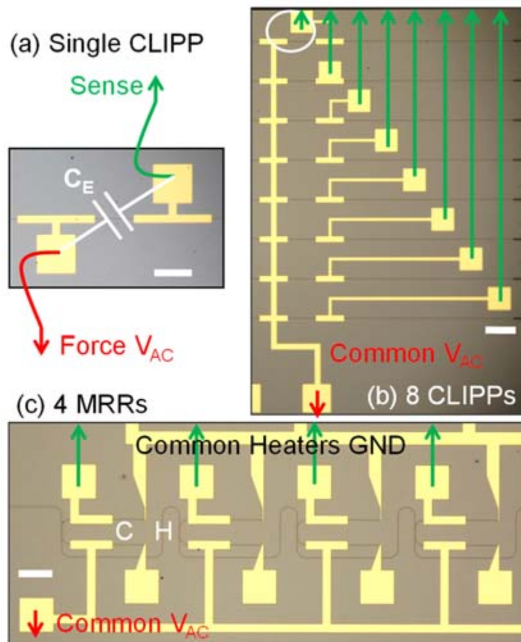

Fig. 6. Guidelines for optimal layout (a) opposite V_{AC} generation and readout bonding wires (red and green lines, respectively) to minimize C_E, (b) sharing of V_{AC} pads for 8 parallel CLIPPs, (c) common V_{AC} and common heater grounds (H) in 4 cascaded MRRs. The scale bar is 100 µm in all the photos.

substrate capacitances C_B and C_{SUB} should be minimized by maximizing t_{BOX} or by choosing a high-resistivity substrate. From an instrumentation point of view, operating above 50 MHz requires a careful electronic design because the impact on the phase delays of the connection cables is no longer negligible. Furthermore, it requires a TIA and a lock-in amplifier with larger bandwidth.

V. Guidelines for Optimal Layout

A. *Inter-electrode capacitance C_E of the bonding wires*

We already introduced in Sec. III.B the spurious capacitance C_E between the two electrodes of the CLIPP. Its presence activates a spurious current in parallel to the signal in R_{WG} which is not modulated by the optical power, thus affecting the measurement. To minimize its value, the “Force” and “Sense” connections to the corresponding electronic inputs should be as far one with respect to the other as possible. If the CLIPP pads are locally placed, as in Fig.6(a), bonding wires may be the major source of C_E. Consider that two bonding wires running parallel from the chip to the electronic board for 1 cm, for example, would contribute for a hundred of fF, giving a high spurious current contribution at the typical working frequencies of 1 MHz. Because of this it is a good practice to direct the bonding wires of the Force and of the Sense electrodes to opposite directions, as sketched in Fig. 6(a).

B. *Routing and minimization of the interconnections*

In optically dense chips [17, 18], where several CLIPP devices are integrated, the bonding pads will likely be aligned along the PIC border. In this case, in addition to the bondings, also the routing from the electrodes to the bonding pads becomes

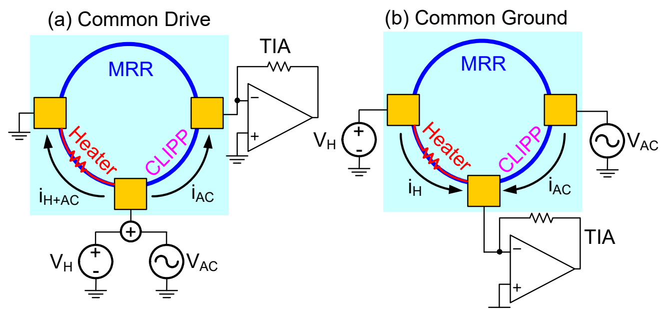

Fig. 7. Comparison between two possible electrode-sharing topologies between the heater and the CLIPP: (a) common driving electrode vs. (b) common ground electrode.

important. First, it would be convenient to share the V_{AC} Force electrodes of all the CLIPP into a single Force pad, thus saving space on the PIC and reducing the number of external bonding wires. Figure 6(b) shows the advantages in terms of area occupation and of bonding connections that a common V_{AC} can bring. Figure 6(c) highlights how a single Force line helps in keeping C_E to a minimum: the V_{AC} signal can be routed to the CLIPPs from a side pad of the PIC, placed well apart from the signal lines and from the pads (lined in the north border of the PIC).

The layout of the Sense lines on the PIC is more relaxed, affecting cross-talk between channels and noise very marginally. In fact the coupling capacitance between channels is indeed small for strips routed parallel at a distance >50µm, indicating that there is a great freedom in the layout to cope with even very dense optical architectures. Also the width of the Sense lines is not critical: it would translate into a capacitance to ground that adds to the TIA input, eventually increasing the TIA noise. As long as the width of these strips is within 5µm, their contribution to the total input capacitance at the TIA (typically of few pF) is indeed negligible.

When dealing with the PIC layout, care should be dedicated to the dummy metal tiles that foundries add to balance the metal fill factor for the etching process. These metal tiles, despite being usually floating, offer a bridge between the electrodes thus increasing the CE, and from the reading electrode towards the grounded substrate, usually increasing the input noise of the amplifier. A non-filling area around the CLIPP is therefore important to avoid these parasitic paths .

C. *Heater-CLIPP Electrode-Sharing Topologies*

In addition to CLIPP, also heaters may share common electrodes when layout simplicity is of concern. Figure 6(c) shows an example in a cascade of 4 MRRs, reducing the required bonding pads from 16 to 10. When space is an issue, as in small size MRR or in Mach-Zehnder interferometer (MZI) [19], one of the electrodes already available to access the heater can be used also to access the CLIPP by profiting that the two signals are spectrally decoupled. As illustrated in Fig. 7, this solution can be implemented in two ways.

In the *common drive* topology (Fig. 7a) the sum of the V_{AC} signal for the CLIPP excitation and the V_H signal for the heater is applied to the middle pad, while the companion pads are separately grounded. The advantage of this scheme is that

the TIA does not need any modification and can be optimized to amplify the CLIPP signal. The disadvantage is that the V_{AC} excitation is applied also across the heater: if the frequency f_{AC} falls within the response bandwidth of the heater (that can reach the MHz range), an undesired modulation can be induced.

In the *common ground* topology (Fig. 7b) the common middle pad is connected to the virtual ground of the TIA and the other pads are used to drive separately the CLIPP and the heater. The price of this solution is a more complex TIA that, in addition to the AC current signal (in the nA range) from the CLIPP, must also handle the large (typically in the mA range) DC current of the heater.

Note that in both configurations the noise of the V_H generator is injected also in the CLIPP path, thus requiring a well filtered V_H generator in order to minimize the noise around f_{AC}. Furthermore, in the common ground configuration the thermal noise of the heater resistor ($4kT/R_{heater}$) is an additional noisy current source to be considered in the design of the TIA. Consequently, if the f_{AC} signal is not excessively perturbing the heater, the common drive configuration is preferable. The common drive solution is also compatible with a wide common ground track for the heaters.

As a last consideration, the minimum distance between the heater and the CLIPP is dictated by the thermal cross-talk. Thermal simulations are required to evaluate the amount and the speed of thermal gradients in the waveguide under the CLIPP during the operation of the heater in the case of highly packed devices [20, 21]. However, given a thermal sensitivity of ~1 nS/°C for the conductance of Si waveguides [4], a few tens of µm of separation are typically enough to make negligible the effect of heaters dissipating tens of mW.

VI. CLIPP Resolution vs Response Time

The response time of the CLIPP is set by the lock-in demodulation bandwidth BW and is governed by the speed-resolution trade-off inherent to all noise-limited measuring systems. By enlarging BW, a faster response is achieved but more noise components are integrated, thus resulting in a worse resolution.

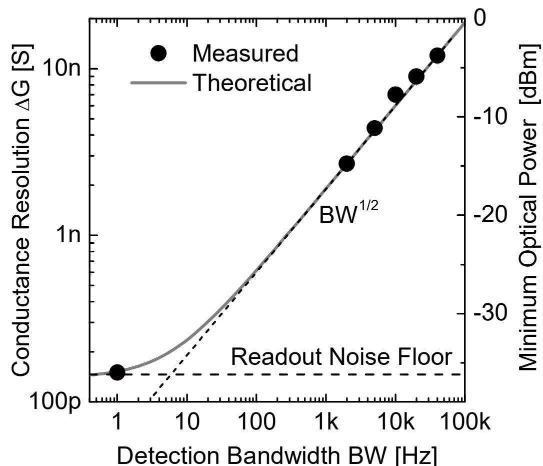

Fig. 8. Diagram showing the bandwidth BW vs. resolution trade-off for a CLIPP of standard size (L = 2D = 200 µm, V_{AC} = 2 V, f_{AC} = 2 MHz). Circles are the experimental points, while the dotted line is the theoretical expectation according to the TIA noise. At high bandwidth the curve increases as ~$BW^{1/2}$.

TABLE II
Summary of CLIPP Design Guidelines

Parameter	Design Rule	Tested values	§
t_{CLA}	Minimize to maximize C_A avoiding additional loss	1 µm	III.A
t_{BOX}	Maximize	2 µm	III.B
$\rho_{substrate}$	Maximize (ideally remove Si)	10Ω cm	III.C
W	Set to w + $2t_{CLA}$	20 µm	IV
L	Maximize, to maximize C_A	100 µm, 200 µm	IV
D	Optimize for a given f_{AC}	100 µm, 200 µm	IV
f_{AC}	Match to the conductance plateau between f_{low} and f_{high}	10 kHz - 10 MHz	IV
C_E	Minimize, optimize layout	< 0.5 pF	V.A

In order to experimentally explore the speed detection limits, the optical power on a straight waveguide is chopper modulated at increasing frequency (up to 10 kHz) and tracked with the CLIPP signal (V_{AC} = 2 V) filtered at correspondingly larger BW from 1 kHz to 40 kHz. Fig. 8 reports the measured minimum detectable signal variation (calculated as 6 times the rms value of the measured noise) as a function of BW.

The experiments confirm that the noise decreases as $BW^{1/2}$ as the BW is decreased (dotted line) and that a optical signal of 30 µW can be detected with a speed of 1 kHz. For very narrow bandwidths (the point at 1 Hz in the figure) other noise sources, in addition to the TIA, come into play, such as the intrinsic limitation of the lock-in detector, setting a lower limit of resolution to around 220 pS in our system. Note that the resolution linearly depends on V_{AC}, which can be increased from the used value of 2 V up to tens of volts if even better resolution than the one in Fig. 8 is desired.

VII. Readout Electronics

In order to minimize the noise in the reading of the waveguide conductance, the total capacitance on the pad connected to the TIA input must be minimized [20]. Therefore, the way in which the electrodes are connected to the electronics is crucial in terms of achievable sensitivity. Coaxial cables should be avoided in the most sensitive applications due to the high capacitance per unit length (6.5 – 10 pF/cm). When a permanent connection is acceptable, bonding wires arranged as described in Sec. III should be preferred to the use of macroscopic spring contacts or microprobes. In order not to jeopardize the benefit of the low-capacitance bonding wires, the length of the connection from the bonding to the TIA input, typically consisting in a copper track on a PCB, should be carefully minimized. To this purpose, the TIA (either an off-the-shelf component [11] or a dedicated ASIC [23]) can be soldered on a small PCB holder hosting at close distance both the photonic chip and the front-end components of the readout chain [10].

The CLIPP readout electronics, comprising the lock-in demodulator, can be implemented in standard CMOS technology, as already demonstrated with a low-noise ASIC

custom-designed to read 32 CLIPPs [23]. The major advantage of an integrated implementation of the readout circuit is the parallelization of several channels in a miniaturized space. This choice becomes mandatory when several tens of CLIPPs need to be simultaneously probed.

The CLIPP technology is suitable for the monolithic integration of both photonics and electronics on the same silicon chip. This scenario would be optimal from the point of view of the minimization of C_E and therefore for the highest possible sensitivity. Analogously, the hybrid solution of bonding a standard CMOS chip on top of a larger photonic chip, such as in the case of copper pillars technology [22], would be suited for the readout of several CLIPPs.

Finally, it must be mentioned that more advanced circuit topologies for current amplifiers can be adopted to loosen the speed-vs-resolution trade-off affecting the basic TIA configuration with resistive feedback, whose degree of freedom is basically the choice of the feedback resistance value. For instance, given the prominently capacitive nature of the CLIPP equivalent impedance, a TIA with capacitive feedback [23] enables achieving frequency independent gain and, at the same time, low-noise (pS resolution) and wide bandwidth (>10 MHz).

VIII. Conclusion

The guidelines given so far to design efficient CLIPP detectors show that transparent monitoring of the optical power in complex integrated photonic circuits is not only a consolidated possibility but is also relatively technology transparent. Indeed, although the results discussed in this work mostly relate to channel Si waveguide realized on silicon-on-insulator platforms, the presented analysis has shown that the key factors in CLIPP behavior depend on basic physical characteristics (a resistive waveguide, an insulating cladding and an accessible metal electrode) present in very different photonic semiconductor based platforms like InP. and others.

Although here the analysis was mostly focused on a ridge waveguide (Fig. 3), the CLIPP is applicable also for rib cross-sections, as we demonstrated with InP [8]. The larger coupling between the top electrode and the waveguide core increases the value of C_A with the beneficial effects discussed above.

The limited area occupied by a CLIPP and the negligible optical loss truly allow placing a significant number of CLIPPs to monitor, tune or lock a complex architecture in very many points of interest. In this case, the paper has presented strategies and design rules for the interconnection layout to fully exploit the CLIPP sensitivity and solutions for footprint reduction based on shared electrodes, together with selection criteria for the read-out electronics. Since all the aspects here discussed are described by quantitative relations, a significant degree of automatization in the choice of the CLIPP parameters during the design phase in an EDA environment [24] is clearly foreseeable.

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