Analytical Modeling of Current Overshoot in Oxide-Based Resistive Switching Memory (RRAM)

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***Abstract*— Current overshoot due to parasitic capacitance during set transition represents a major concern for controlling the resistance and current consumption in resistive switching memory (RRAM) arrays. In this letter, the impact of current overshoot on the low-resistance state (LRS) is evaluated by means of experiments on one-transistor/one-resistor structures of HfO_2 RRAM. We develop a physics-based analytical model, able to calculate the LRS resistance and the corresponding reset current by a closed-form formula. The model allows predicting the current overshoot impact for any value of compliance current, set voltage, and parasitic capacitance.**

***Index Terms*— Resistive switching memory, RRAM, capacitive overshoot, reliability, analytical modeling, non volatile memory.**

I. Introduction

RESISTIVE switching memory (RRAM) is a promising candidate for next-generation non-volatile memory and storage class memory [1]. RRAM offers high speed [2], high endurance [3] and good scaling thanks to atomic-scale conductive filament (CF) [4]. Reliability of RRAM is mostly affected by switching variability [5], low-frequency noise resulting in distribution broadening [6] and current overshoot during set transition [7]–[15]. The latter arises due to the parasitic capacitance C_P, causing an additional discharge/charge current in the RRAM device even when the compliance current I_C is limited by a series transistor. Since C_P contains contributions from the bitline/wordline capacitances, overshoot effects play a major role in the power consumption and reliability of large RRAM arrays. Therefore, predicting and controlling the impact of the current overshoot is essential in the design of RRAM arrays.

In this letter, we present an analytical formula for the impact of C_P on resistance and reset current I_{reset}. The model predicts the impact of the set voltage and I_C on overshoot. Our results support the ability of the model to accurately predict overshoot effects for RRAM at any arbitrary value of C_P, thus providing a valuable tool to evaluate the impact on large RRAM arrays.

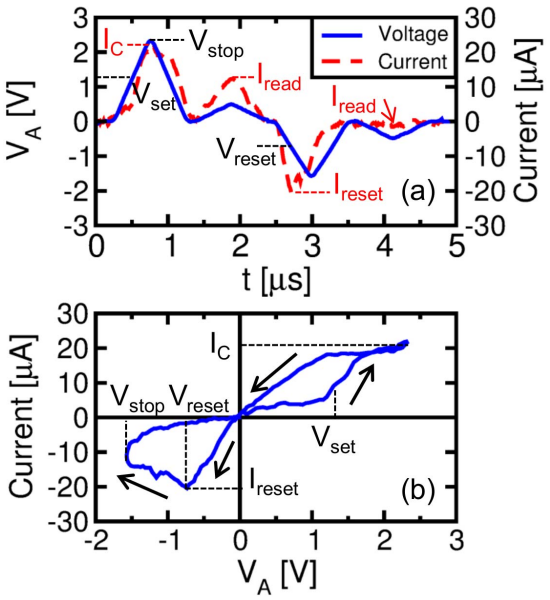

Fig. 1. Voltage and current experimental measurements for one cycle including set and reset processes and the corresponding read pulses (a), and the corresponding I-V curve (b). Definitions of V_{set}, V_{reset}, V_{stop}, I_C and I_{reset} are reported in the figure.

II. Experimental Results

We characterized switching and overshoot effects in Si-doped HfO_x RRAMs with a TiN bottom electrode (BE) and a Ti top electrode (TE) [16]. Devices were integrated in a 1-transistor/1-resistor (1T1R) structure to provide control of I_C and minimize C_P in parallel to the RRAM device. The parasitic capacitance includes contributions from the drain capacitance of the transistor, and the connecting metal line between transistor and RRAM. In a RRAM array, C_P might also include the bitline/wordline capacitance. Experiments were conducted by applying voltage pulses to the gate electrode and the TE with an arbitrary waveform generator, while TE voltage and current in the MOSFET were monitored by an oscilloscope. Fig. 1 shows the typical result of the pulsed characteristics of our RRAM device. Fig. 1a shows the applied TE voltage during an individual cycle including set and reset pulses, each followed by a read pulse to probe the resistance state. Each pulse had a duration $t_P = 1\ \mu s$.

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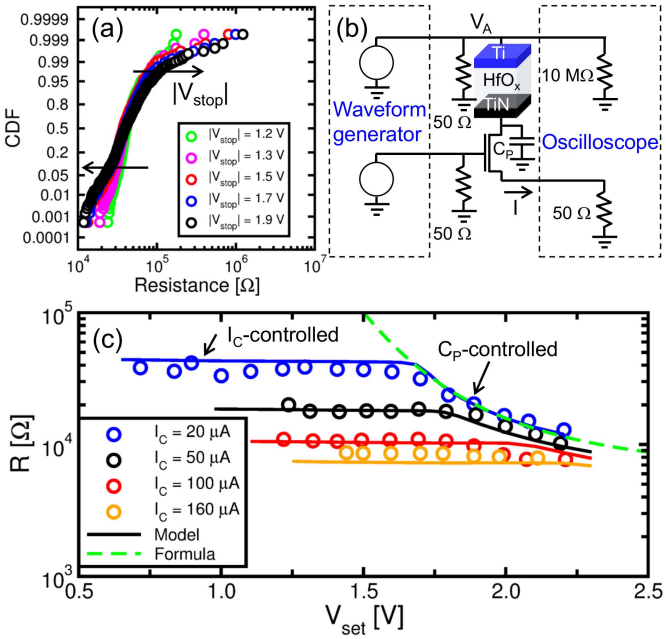

Fig. 2. Experimental cumulative distributions of LRS for increasing $|V_{stop}|$ (a), schematic illustration of the 1T1R circuit with parasitic capacitance (b), and average LRS resistance as a function of V_{set} from data and calculations. For high $|V_{stop}|$, a low resistance tail due to parasitic overshoot appears in (a), together with a high resistance tail due to non-switching events. Calculations from a device compact model and the analytical Eq. (5) well agree with data in the C_P-controlled region in (c).

The dashed line displays the measured current revealing set/reset processes. A set transition to the low-resistance state (LRS) appears during the set pulse, followed by a read pulse of 0.5 V. The subsequent reset pulse causes the reset transition to the high resistance state (HRS), measured by a second voltage pulse of −0.5 V. Note the significantly different I_{read} after set ($I_{read} \approx 10\ \mu$A) and after reset ($I_{read} \approx 0$). Fig. 1b shows the corresponding I-V curve extracted from Fig. 1a. I_C was equal to 20 μA in the experiment in Fig. 1b by control of the gate voltage $V_G = 1.2$ V in the transistor. The set voltage $V_{set} \approx 1.3$ V is marked by the transition to the LRS. Reset transition takes place at about −0.8 V with a reset current $I_{reset} \approx 20\ \mu$A, close to I_C [17]. Note that V_{set} corresponds to the V_A able to induce a set transition in the device, thus it is applied to the whole 1T1R structure. We used triangular pulses to extract V_{set} and V_{reset}, however, similar results could be obtained for pulses with other shapes.

III. Parasitic Overshoot

We cycled RRAM cells for 1000 cycles, then we extracted the cumulative distribution function (CDF) of the LRS resistance. Results are shown in Fig. 2a, for increasing $|V_{stop}|$. The CDF shows tails at high and low resistance, both increasing with $|V_{stop}|$. The high resistance tail is due to non-switching events, where the device could not switch, or could switch only partially, due to the relatively large value of V_{set}. As $|V_{stop}|$ increases, the reset transition results in a deeper HRS with a relatively large V_{set}, which thus causes increasing high-resistance tail in the LRS distribution. On the other hand, the low resistance tail is due to the current overshoot

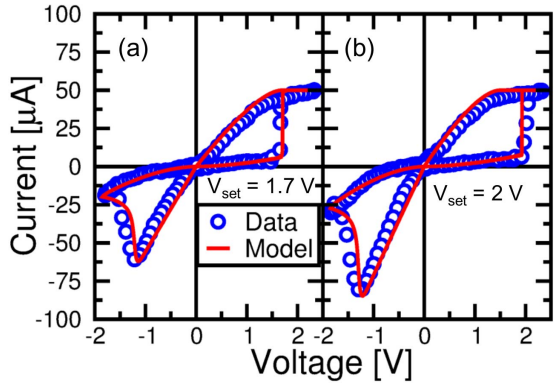

Fig. 3. Experimental and calculated I-V curves for different $V_{set} = 1.7$ V (a) and 2 V (b). Increasing V_{set} leads to decreasing LRS resistance hence higher $|I_{reset}|$.

resulting from C_P connected to the node between RRAM and MOSFET, as shown in Fig. 2b. The capacitive current across C_P causes a transient excess current higher than the nominal I_C during set transition. The capacitive current is due to the sudden increase of the potential across C_P as the 1T1R voltage divider is changed by the set transition. The extra-current induced by C_P charging, in combination with the relatively large V_{set} accelerating ion migration, leads to a CF overgrowth, with a subsequent lower LRS resistance in correspondence of the LRS low-resistance tail. As $|V_{stop}|$ increases, HRS resistance and V_{set} increase, thus causing larger overshoot effects due to the exponential increase of ion migration rate with voltage [17], [18]. The low-resistance tail at increasing V_{stop} in Fig. 2a can thus be attributed to the overshoot arising for large V_{set}.

Fig. 2c shows the correlation between the average value of the LRS resistance as a function of V_{set} in the preceding set operation, for $I_C = 20\ \mu$A, 50 μA, 100 μA and 160 μA. At low $V_{set} < 1.5$ V, the LRS resistance shows a constant value, which increases at decreasing I_C, namely an I_C-controlled regime. For higher V_{set}, the LRS resistance decreases with V_{set} revealing the effect of the current overshoot, namely the C_P-controlled regime.

Results are reproduced by simulations of the set transition in a 1T1R structure using a compact model of the RRAM [19] assuming $C_P = 30$ fF. The compact model in [19] was demonstrated for RRAM devices under various set/reset conditions and for simple RRAM circuits [20], [21]. In the simulations, V_{set} is adjusted by assuming variable resistance in the HRS, which is naturally obtained in the experiment thanks to the stochastic switching in our RRAM [5]. Fig. 3 reports the impact of capacitive overshoot at variable V_{set}, showing the measured and calculated I-V curves for relatively low $V_{set} = 1.7$ V (a) and high $V_{set} = 2$ V (b). In both cases, I_C was fixed to $I_C = 50\ \mu$A. For $V_{set} = 1.7$ V, current overshoot is negligible as the CF growth time is comparable or longer than the RC constant, thus the voltage across C_P is readjusted before or during CF growth. On the other hand, Fig. 3b shows that for $V_{set} = 2$ V, LRS resistance reaches a lower value due to the CF growth time being shorter than the RC time. The lower resistance is reflected by a larger I_{reset} in the subsequent reset operation, further supporting the evidence

of a CF overgrowth. Since $I_C \approx I_{reset}$, an effective overshoot current during set transition around 80 μA can be estimated from Fig. 3b. The compact model accounts for the observed values of LRS resistance and I_{reset}.

IV. Analytical Model of Overshoot Effects

To predict the LRS resistance as a function of V_{set} and C_P, we consider the growth rate of the CF diameter ϕ given by [17]:

$$\frac{d\phi}{dt} = Ae^{-\frac{E_A - aqV}{k(T_0 + \frac{V^2}{8\rho k_{th}})}}, \quad (1)$$

where $A = 200$ ms^{-1} is a pre-exponential factor, $E_A = 1.28$ eV is the energy barrier for ion migration, $\alpha = 0.3$ [22] is a barrier lowering coefficient, k is the Boltzmann constant and V is the applied voltage. Joule heating is described by the denominator in the exponent, where T_0 is the ambient temperature, ρ and k_{th} are the effective resistivity and thermal conductivity, with values $\rho = 1.97$ mΩcm and $k_{th} = 7$ Wm$^{-1}K^{-1}$. The exponential dependence of switching speed on voltage in Eq. (1) is similar to other proposed models in the literature for migration-based switching in RRAM [17], [22]–[28]. Different models describing CF restoration during set transition lead to the same qualitative behavior, provided that an exponential voltage acceleration is assumed for the set process. Assuming that the voltage across the device is kept constant by C_P during CF growth, we can estimate the CF diameter ϕ_{LRS} after set process by integrating Eq. (1), namely:

$$\phi_{LRS} = \int_0^{\tau_{set}} \frac{d\phi}{dt} dt = Ae^{-\frac{E_A - aqV_{set}}{k(T_0 + \frac{V_{set}^2}{8\rho k_{th}})}} \tau_{set}, \quad (2)$$

where τ_{set} is the effective set time. The latter can be approximated by the RC time constant in the C_P-controlled overshoot regime in Fig. 2c, namely:

$$\tau_{set} = RC_P, \quad (3)$$

where R is the LRS resistance which can be calculated approximating the CF shape by a cylinder, thus leading to:

$$R = \rho \frac{L}{\frac{\pi}{4}\phi_{LRS}^2}, \quad (4)$$

where $L = 5$ nm is the CF length. By substituting Eq. (3) and (4) in Eq. (2), we obtain

$$R = \left(\frac{4\rho L}{\pi A^2}\right)^{1/3} e^{\frac{E_A - aqV}{k(T_0 + \frac{V_{set}^2}{8\rho k_{th}})}} C_P^{-2/3}, \quad (5)$$

which directly yields R as a function of C_P and V_{set} in the C_P controlled regime. From Eq. (5), I_{reset} can be estimated as $I_{reset} = V_{reset}/R$, where V_{reset} is a characteristic constant for a given pulse width [17]. It can be noticed that R does not depend on I_C, but follows a universal behavior, in agreement with data in Fig. 2c. The results of the analytical formula are plotted in Fig. 2c, showing a good agreement with data and with the compact model in the C_P-controlled region. Eq. (5) applies to the C_P-controlled region, where the overshoot transient takes place in a time τ_{set} which is generally much smaller than the actual pulse width t_P. For instance, for $R = 10$ kΩ and $C_P = 100$ fF, one obtains $\tau_{set} = 1$ ns, hence much shorter than t_P. Therefore, we do not expect any significant change of Eq. (5) at variable t_P, at least for $t_P > 1$ ns.

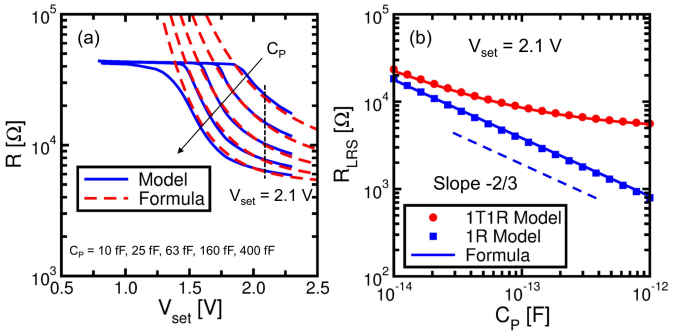

Fig. 4. Calculated R from the compact model [19] and from the formula in Eq. (5) as a function of V_{set} for different C_P, from 10 fF to 400 fF (a). (b) shows the 1T1R and 1R resistances versus C_P at a constant $V_{set} = 2.1$ V, as shown in (a). Results show a complete agreement, with a slope -2/3 of the 1R resistance.

V. Discussion

In our work the parasitic capacitance $C_P = 30$ fF is consistent with the drain-capacitance of the transistor in the 1T1R with possible contributions from the metal interconnect. On the other hand, the capacitive load in high-density memory circuits might be significantly larger than $C_P = 30$ fF as a result of, e.g., long bitlines in a crossbar array. To assess the impact of C_P, Fig. 4a shows the calculated R as a function of V_{set} for increasing C_P, from 10 fF to 400 fF. Results from Eq. (5) are compared to simulations as in Fig. 2 and 3. The onset of the C_P-controlled regime is anticipated at increasingly low V_{set} for increasing C_P, as a result of the $C_P{}^{-2/3}$ dependence in Eq. (5). Note the saturation of the LRS resistance equal to 4.7 kΩ for high V_{set} due to the series resistance of the transistor. The formula accounts very well for the R behavior in the C_P regime, even for a wide C_P range of almost 2 decades.

To further assess the validity of Eq. (5), we evaluated the LRS resistance as a function of C_P for a constant $V_{set} = 2.1$ V, as indicated in Fig. 4a. Fig. 4b shows the 1T1R compact model resistance and the corresponding 1R compact model resistance of the RRAM (i.e., without the series resistance of the transistor) as a function of C_P. The computed results from Eq. (5) are also shown for comparison, in good agreement with simulations. In particular, the 1R resistance shows a slope $-2/3$ on the log-log plot, as expected from the $C_P{}^{-2/3}$ term in Eq. (5).

VI. Conclusion

We studied current overshoot affecting the set transition at high V_{set} in RRAM devices. An analytical formula is presented to easily predict LRS resistance as a function of V_{set}, C_P and other microscopic parameters in the device. Our analysis suggests that current overshoot can be minimized by accurately controlling V_{set} and its variability, and by limiting C_P and the switching speed of the RRAM.

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