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Organic integrated circuits for information storage based on ambipolar polymers and charge injection engineering

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Ambipolar semiconducting polymers, characterized by both high electron (μ_e) and hole (μ_h) mobility, offer the advantage of realizing complex complementary electronic circuits with a single semiconducting layer, deposited by simple coating techniques. However, to achieve complementarity, one of the two conduction paths in transistors has to be suppressed, resulting in unipolar devices. Here, we adopt charge injection engineering through a specific interlayer in order to tune injection into frontier energy orbitals of a high mobility donor-acceptor co-polymer. Starting from field-effect transistors with Au contacts, showing a p-type unbalanced behaviour with $\mu_h = 0.29$ cm^2/V s and $\mu_e = 0.001$ cm^2/V s, through the insertion of a caesium salt interlayer with optimized thickness, we obtain an n-type unbalanced transistor with $\mu_e = 0.12$ cm^2/V s and $\mu_h = 8 \times 10^{-4}$ cm^2/V s. We applied this result to the development of the basic pass-transistor logic building blocks such as inverters, with high gain and good noise margin, and transmission-gates. In addition, we developed and characterized information storage circuits like D-Latches and D-Flip-Flops consisting of 16 transistors, demonstrating both their static and dynamic performances and thus the suitability of this technology for more complex circuits such as display addressing logic. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4871715]

There is a growing interest towards the exploitation of organic electronics in fields ranging from large-area and flexible circuits and detectors[1,2] to chemical[3] and bio-sensors.[4] A particularly strong driving force comes from display industry for which high performing organic field-effect transistors (OFETs), suitable for active matrix display addressing, are required besides flexible and/or transparent backplanes. This raised the need to devise viable approaches for the integration of organic transistors into robust integrated circuits (ICs), especially for logic applications.[5] To guarantee good immunity to signal variations and low power dissipation n- and p-type transistors have to be integrated on the same substrate: in silicon-based electronics this approach, termed complementary metal-oxide-semiconductor technology (CMOS),[6] is responsible for the excellent performance and reliability of silicon-based logic circuits. In addition, a complementary-like organic technology has to adopt solution processable materials to guarantee the capability to adopt cost-effective deposition techniques, inherited from graphical arts, which enable printing electronics on large area.[7]

There has been an increasing number of reports showing solution-processed, OFETs-based complementary transistors and circuits.[8–11] One of the most commonly adopted methods to fabricate a fully complementary circuit is semiconductor patterning,[12] which uses two different semiconductors for the two different transistor types. Although this appears as a straightforward approach, it implies a many-steps fabrication process with various technological constraints. For example, different fabrication steps and processing parameters needed to optimize charge transport in one of the two semiconductors (e.g., annealing temperatures) may easily lead to a non-optimised transport in the other. This may result in a large difference in the mobility for holes and electrons, therefore requiring large and not practically viable width ratios between the n- and p-type transistors in order to balance the complementary logic and preserve high noise margins (NMs).[13] Moreover, semiconductor patterning is strictly dependent on the minimum feature size set by the adopted deposition technique, leading to inefficient interconnects routing or to low device density circuits. The latter is in an opposite trend with respect to the efforts of channel length scaling.[14] For these reasons, the use of a single ambipolar polymer, showing balanced hole and electron mobility, for the fabrication of complementary organic ICs, has been recently proposed.[15–17] The use of a single semiconductor for both kind of transistors perfectly matches the requirements of all those printing techniques commonly used for the development of large area organic devices, thus making ambipolar semiconductors a promising choice for the simplification of complementary organic ICs manufacturing.

However, performance of complementary electronic circuits based on ambipolar devices are poor in terms of noise

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margin and power dissipation because, in an ideally ambipolar transistor, the application of a gate voltage that lowers the density of one charged species accumulated in the channel will inevitably increase the density of the opposite one. Therefore, transistors cannot be totally turned off,[7] resulting in a loss of performance and robustness.

As a general strategy to solve this issue, part of the authors have recently proposed a technique[18] to obtain truly complementary logic circuits based on high-performance ambipolar polymers by unipolarizing otherwise ambipolar devices, thanks to the insertion of a suitable charge injection layer (CIL). The CIL serves a twofold role: (i) optimizing the injection of a specific charge species by inducing a more favourable alignment of the electrode work function with the corresponding frontier molecular orbital, and (ii) consequently suppressing the injection of the other carrier. The correct engineering of the charge injection barriers for holes and electrons can thus be adopted to turn ambipolar OFETs into unipolar devices. Specifically, it has been demonstrated that, in combination with high-mobility donor-acceptor co-polymers,[18] gold electrodes can be used to fabricate p-type devices with suppressed apparent electron mobility, while it is possible to take advantage of the strong hole blocking and electron injection properties of caesium salts in order to induce comparable n-type behaviour. Although the CIL has to be patterned, thus requiring an additional patterning fabrication step, it is a much less delicate process than semiconductor patterning.

In this work, we adopt the charge injection engineering technique to demonstrate its general suitability for complex integrated and complementary logic circuits, such as Flip-Flops, based on ambipolar polymers OFETs. To achieve this, we have adopted the poly(thienylenevinylene-*co*-phthalimide) with an ethylhexyl substituent (PTVPhI-Eh, Fig. 1(a)), a donor-acceptor co-polymer showing good hole and electron mobilities up to ~0.9 $cm^2/V\,s$ and ~0.2 $cm^2/V\,s$, respectively. Upon optimization of a caesium fluoride injection layer for unipolar n-type transistors, and by using bare gold electrodes to obtain unipolar p-type transistors, we have implemented a complementary pass-transistor logic, which minimizes the number of transistors needed for the logic gates. We have first demonstrated properly working inverters, pass-transistors, and D-Latches.[13] These building blocks are then integrated to realize edge-triggered D-Flip-Flops,[13] which are fundamental logic elements featuring an information storage functionality, each comprising 16 OFETs. Flip-Flops are the basis of more complex circuits and electronic systems, such as shift-registers, decoders, encoders, and driving circuits for organic photodetectors arrays and displays, therefore demonstrating the suitability of the adoption of a single ambipolar polymer for the development of future ICs.

We adopted top-gate bottom-contact (TG/BC) structure for our devices (Fig. 1(b)), a staggered architecture which can reduce the contact resistance effect.[19] A 35 nm thick Au source and drain contacts, on top of a 1.7 nm thick Cr adhesion layer, were patterned on a thoroughly cleaned low alkali 1737F Corning glass substrate through a standard lithographic lift-off process. Contacts for single transistors had a channel width to length ratio (W/L) of 10 000 μm/20 μm; for logic gates and circuits, the channel length was kept constant, while W was varied to compensate the mobility difference between p-type and n-type transistors, resulting in a W/L for the p-type of 2000 μm/20 μm and a W/L for the n-type of 6000 μm/20 μm. As an electron-injection layer for this work, we used CsF, which gave the best results in terms of unipolarization.[20,21] Before CsF deposition, substrates were rinsed with acetone and isopropyl alcohol. The deposition of the CsF charge injection interlayer is performed only on transistors to be n-type unipolarized; to this end, CsF is

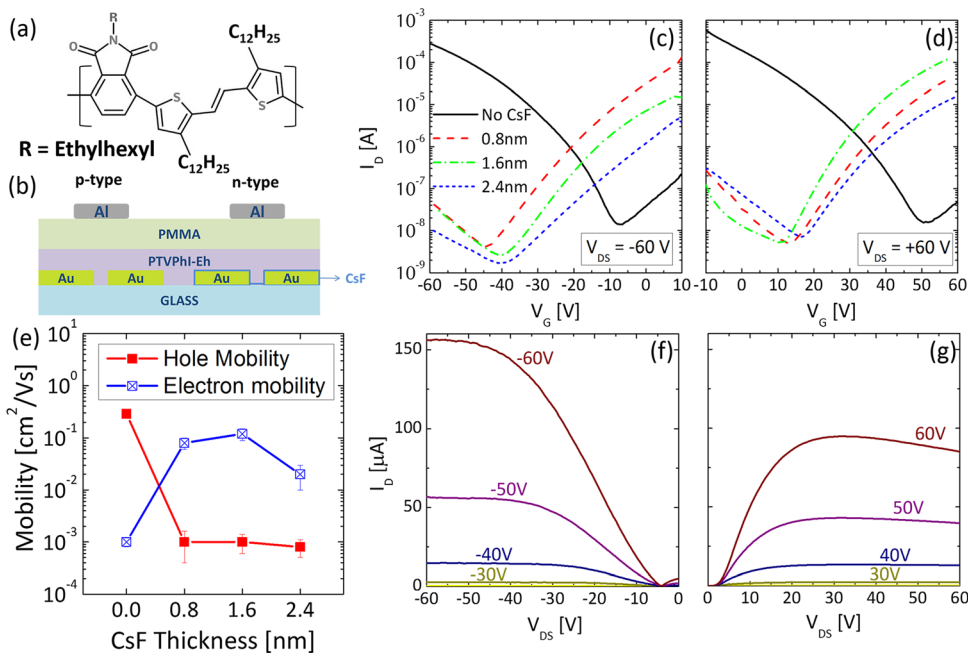

FIG. 1. (a) Chemical structure of the PTVPhI-Eh adopted in this study and (b) schematic cross-section of the OFET. (e) Holes and electron mobilities for different CsF film thickness by thermal evaporation, all values are calculated at $|V_G| = |V_D| = 60$ V. Transfer curves for different CsF thickness in (c) hole accumulation regime and (d) electron accumulation regime. Output curves for (f) p-type untreated contacts transistor and (g) n-type unipolarized device with optimized CsF thickness of 1.6 nm. All transistors have $W_p/L_p = W_n/L_n = 10$ mm/20 μm.

thermally evaporated through a metal shadow mask. After the evaporation, samples are annealed at a temperature of 120 °C for 30 min. The ambipolar polymer PTVPhI-Eh was deposited in a nitrogen atmosphere from a 10 mg/ml anhydrous chlorobenzene solution by spin-coating at 2000 rpm for 60 s to obtain a ~40 nm thick film. The semiconductor film was then annealed at 200 °C for 20 min to guarantee solvent drying and optimal charge transport properties.[15] Poly(methyl-methacrylate) (PMMA, $M_w = 120\,000$, Sigma-Aldrich) was adopted as the dielectric layer, and deposited by spin-coating from a 80 mg/ml *n*-butyl acetate solution. A thickness of 500 nm was optimized for the discrete device by spinning at 1800 rpm for 60 s. For the integrated circuits, a 600 nm thick dielectric film was adopted by spinning at 1250 rpm for 60 s. After the deposition of the dielectric, samples were annealed at 80 °C for 30 min. Via-holes for circuit inter-layer interconnections were fabricated via chemical drilling by ink-jet printing of chlorobenzene. A 50 nm thick aluminium layer was thermally evaporated through a metal shadow mask to fill the via-holes and pattern the gate electrodes. Characterizations of discrete transistors, logic ports, and circuits were performed in an inert nitrogen atmosphere; measurements of the transistors characteristic curves and of the inverters voltage transfer characteristics (VTC) were performed by mean of an Agilent B1500A Semiconductor Parameter Analyzer. The dynamic response of circuits was measured using a Tektronix P5122 high impedance probe with low parasitic capacitance connected to a Tektronix DPO2014 Oscilloscope, this configuration ensures a load capacitance of ≈4.6 pF. Moreover, the use of such probe eliminates the need for output buffers in the circuit layout. Input signals and voltage supply were applied to the circuits by an FLC Electronics Multichannel WFG600 High-Voltage Waveform Generator.

OFETs based on PTVPhI-Eh behave as p-type devices by adopting bare Au electrodes[18] because Au source and drain electrodes work-function W_F, in the range of 4.7–5.3 eV,[15] well matches with the HOMO level (~5.2 eV (Ref. 15)) of the polymer. In the same devices electron injection is impeded by a high energetic barrier caused by the LUMO level of ~3.4 eV.[15] The resulting OFET transfer characteristics in hole-accumulation regime (Fig. 1(c)) shows in fact a strongly unbalanced ambipolar behaviour in favour of holes, with an extracted hole mobility (μ_h) in saturation ($|V_{GS}| = |V_{DS}| = 60$ V) of 0.29 ± 0.03 cm^2/V s. Device measurements in the electron-accumulation regime instead (Fig. 1(d)) highlight a poor n-type behaviour, with an apparent electron saturation mobility (μ_e) of 0.001 cm^2/V s ($V_{GS} = V_{DS} = 60$ V). In order to obtain suitably matched n-type devices, we have first investigated the electron injection properties in devices with CsF injection layer by varying the CIL thickness from 0.8 nm to 2.4 nm. The thickness of the CsF films were chosen in order to balance the reduction in electrode W_F, owing to its strong interfacial dipole moment,[18] and the electrically insulating properties of CsF thick layers.[21] The OFETs transfer characteristics in hole-accumulation regime (Fig. 1(c)) show that the insertion of CsF interlayer causes a strong decrease in hole current, thus validating the hole-blocking function of these salts, resulting in a minimum apparent hole mobility of $\mu_h \approx 8 \times 10^{-4}$ cm^2/V s with 2.4 nm-thick CsF film. With respect to bare electrodes, functionalized ones produce an enhancement in electron injection for all the thicknesses taken into account, with an optimum for 1.6 nm resulting in an electron mobility μ_e of 0.12 ± 0.03 cm^2/V s. By increasing the film thickness above 1.6 nm, a decrease of apparent electron injection, attributed to the CsF insulating behaviour, is observed. A comparison between the device parameters extracted with the different deposition thickness is shown in Fig. 1(e). The output characteristics for single devices optimized for p-type behaviour, i.e., with untreated Au electrodes, and for the n-type behaviour, i.e., with a 1.6 nm interlayer, are shown in Figs. 1(f) and 1(g), respectively. The output curves reflect the ratio between hole and electron mobilities ($\mu_h/\mu_e = 2.4$), resulting in a p-type to n-type current ratio of 2.2.

These results enable the design of real complementary logic: patterning of CsF allows to integrate p-type transistors with $\mu_h = 0.29 \pm 0.03$ cm^2/V s and n-type transistors with $\mu_e = 0.12 \pm 0.03$ cm^2/V s on the same substrate. We chose to develop complementary circuitry based on pass-transistor logic as the best trade-off between device number per logic function and logic robustness. The main building blocks for this logic family are inverters and transmission gates (TGTs), the first ones acting as logic inversion elements, while the second ones acting as logic switches.

Both static and dynamic characterizations of the complementary inverter (Fig. 2(a)), integrating the p- and n-type optimized devices, were performed in order to verify the logic robustness. To properly design logic inverters with a threshold voltage equal to half of the supply voltage ($V_{DD}/2$), property required for high noise margins and logic robustness, the moderate current mismatch between n- and p-type transistors, originated by the difference in mobility and threshold voltages, was balanced acting on the transistor channel widths, making $W_n = 3W_p$ while keeping a constant channel length of $L = 20\,\mu$m. The tuned logic threshold turned out to be 36.6 ± 3.2 V at $V_{DD} = 70$ V with a 2.2% mean error compared to the ideal value (Fig. 2(b)).

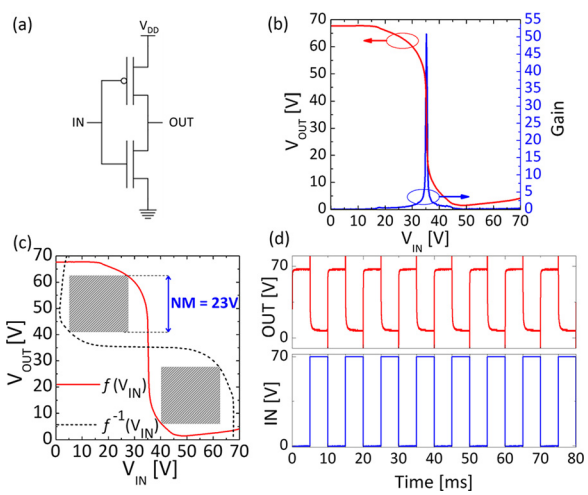

FIG. 2. (a) Complementary inverter circuit layout based on PTVPhI-Eh OFETs and (b) its VTC. (c) Noise margin calculation and (d) dynamic response to a 100 Hz square wave. Aspect ratios of transistors are $W_p/L_p = 2$ mm/20 μm and $W_n/L_n = 6$ mm/20 μm.

Moreover, the VTC shows a quasi rail-to-rail behaviour and a high gain of ≈52 measured as the first derivative of the VTC in correspondence with the logic threshold voltage. NM calculation was performed according to the maximum equal criterion (MEC).[22] The NM is found to be 23 V at $V_{DD} = 70$ V, which is 65.7% of $V_{DD}/2$, thus exceeding the minimum value required for proper circuit operation ($NM_{MIN} = 10\%$)[23] (Fig. 2(c)). Dynamic response to a 100 Hz input square waveform is shown in Figure 2(d). A detailed view of the rising edge of the output waveform (Fig. SM4),[24] allows to extract a 10%–90% rise-time $t_{rise} = 34.2\ \mu$s. The extraction takes into account the maximum quasi-static voltage dynamic (≈63 V, extracted from the inverter VTC in Fig. 2(b)) and the input-output signal capacitive feed-through due to the gate-to-drain capacitances, which induces 36 V spikes on the output node that deeply influence the circuit speed. The rise-time value allows us to expect proper logic inversion up to the kHz regime (Fig. SM5).[24] Further efforts are ongoing in order to enhance the circuit speed, acting on crucial parameters such as channel length, semiconductor mobility, and parasitic capacitances.

The second building block of the pass-transistor logic is the transmission gate (Fig. 3(a)), consisting of two transistors connected in parallel (one p-type and one n-type) that share the source and drain electrodes and are driven by a clock signal and its complementary, respectively (from now on referred to as CK and CK′). A fully ambipolar approach cannot be adopted for this building block; a non-switched-off device would lead the TGT to act as a short circuit between source and drain for any biasing condition. Instead, the unipolarization approach perfectly suits the requirements for this logic gate. Thanks to the developed unipolarized transistors, we have demonstrated correct logic behaviour of the transmission gate through dynamic characterizations (Fig. 3(b)) by feeding a 100 Hz triangular waveform to the input of the transmission gate and by recording the waveforms at the output node with the high-impedance probe already mentioned. When CK is high (CK' low) both n- and p-type transistors are ON and the output follows the input voltage, the transmission gate acts as a short circuit with a relatively small resistance between source and drain contacts through the transistor ON resistance (Fig. 3(b)). On the contrary, when CK is low (CK′ high), both transistors are OFF and only a feed-through signal through the structure's stray capacitances is present. However, the amplitude of this signal is negligible with respect to the noise margin, and cannot produce a logic fault in the successive logic gate.

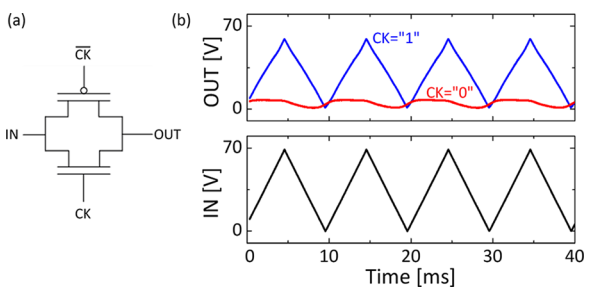

FIG. 3. (a) Transmission gate circuit layout and (b) dynamic behaviour for different clock states with a 100 Hz triangular wave. Aspect ratios of transistors are $W_p/L_p = 2$ mm/20 μm and $W_n/L_n = 6$ mm/20 μm.

Once demonstrated the proper behaviour of the pass-transistor logic building blocks, we have integrated them into a more complex logic circuit design, namely, edge-triggered D-Flip-Flop consisting of 16 transistors (Fig. 4(a)). A Flip-Flop[8,25–29] is a clock-controlled memory element used as a basic component for memory circuits and registers; it stores the input state (data) and adjusts the device output according to the stored state only in response to the clock signal transition. We developed a master-slave D-Flip-Flop by connecting in series two D-Latches (further details in the supplementary material[24]) with opposite transparency periods. In the circuit implemented here, the input data are sampled and brought to the output on the clock's falling edge, making this logic block negative-edge triggered. Output waveform (Fig. 4(c)) shows that the logic state of the input data is sampled at the falling edge of the clock, whereas the block is not transparent in between successive negative clock transitions, meaning that the output state remains unchanged despite input data changes its value.

In summary, we have investigated the possibility to adopt a single ambipolar semiconductor to develop true complementary logic by means of the unipolarization approach through charge injection engineering. P-type transistors with hole mobility $\mu_h = 0.29$ cm^2/V s were fabricated by using bare Au gold contacts, showing good hole injection properties in PTVPhI-Eh. N-type devices with $\mu_h = 0.12$ cm^2/V s mobility were obtained by tuning electron injection through

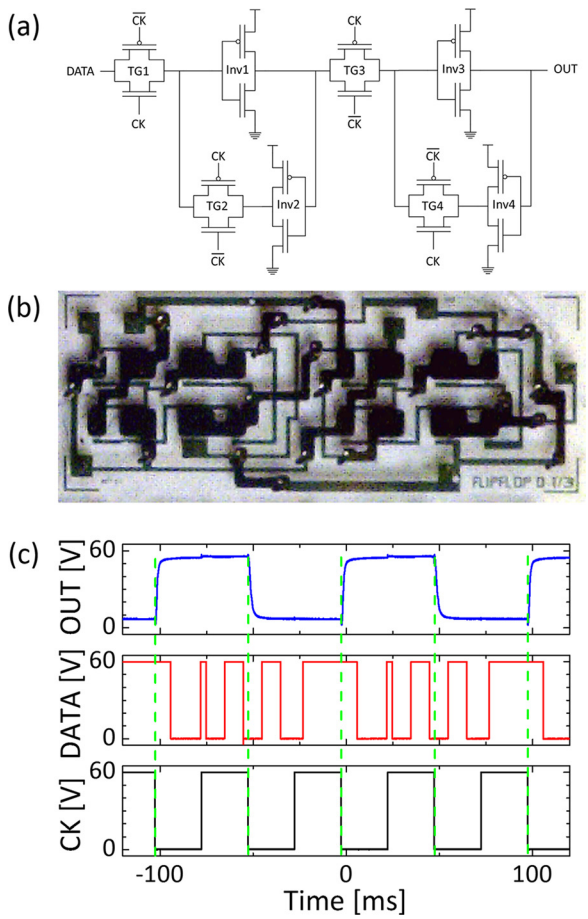

FIG. 4. Quasi static negative edge triggered D-Flip Flop circuit layout (a), optical microscope picture of the circuit (b) and dynamic behaviour with a 20 Hz clock signal and random data input (c).

a CsF interlayer, which resulted in an optimum thickness of 1.6 nm. The complementary devices enabled the demonstration of logic inverters and transmission gates, which were then integrated in a D-Flip-Flop comprising 16 transistors. Our results show that ambipolar polymers unipolarized through charge injection engineering are very promising for complex logic circuitry like shift-registers and for fundamental logic functionalities required for the adoption of organic integrated circuits in real applications.

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